# P6450
# Logic Analyzer Probe with D-Max™ Probing Technology

## Instruction Manual

**Revision A**

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

**Warning**

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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- In North America, call 1-800-833-9200.
- Worldwide, visit www.tektronix.com to find contacts in your area.

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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[W2 – 15AUG04]

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# General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

*Only qualified personnel should perform service procedures.*

While using this product, you may need to access other parts of a larger system. Read the safety sections of the other component manuals for warnings and cautions related to operating the system.

## To Avoid Fire or Personal Injury

**Connect and disconnect properly.** Connect the probe output to the measurement instrument before connecting the probe to the circuit under test. Connect the probe reference lead to the circuit under test before connecting the probe input. Disconnect the probe input and the probe reference lead from the circuit under test before disconnecting the probe from the measurement instrument.

**Ground the product.** This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

**Observe all terminal ratings.** To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

The inputs are not rated for connection to mains or Category II, III, or IV circuits.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

**Power disconnect.** The power cord disconnects the product from the power source. Do not block the power cord; it must remain accessible to the user at all times.

**Do not operate without covers.** Do not operate this product with covers or panels removed.

**Do not operate with suspected failures.** If you suspect that there is damage to this product, have it inspected by qualified service personnel.

**Avoid exposed circuitry.** Do not touch exposed connections and components when power is present.

**Use proper fuse.** Use only the fuse type and rating specified for this product.

**Do not operate in wet/damp conditions.**

**Do not operate in an explosive atmosphere.**

**Keep product surfaces clean and dry.**

**Provide proper ventilation.** Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

## Terms in This Manual

These terms may appear in this manual:

**WARNING.** *Warning statements identify conditions or practices that could result in injury or loss of life.*

**CAUTION.** *Caution statements identify conditions or practices that could result in damage to this product or other property.*

## Symbols and Terms on the Product

These terms may appear on the product:

- DANGER indicates an injury hazard immediately accessible as you read the marking.
- WARNING indicates an injury hazard not immediately accessible as you read the marking.
- CAUTION indicates a hazard to property including the product.

The following symbol(s) may appear on the product:

CAUTION
Refer to Manual

Earth Terminal

Chassis Ground

# Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

**Do Not Service Alone.** Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

**Disconnect Power.** To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

**Use Care When Servicing With Power On.** Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

# Compliance Information

This section lists the EMC (electromagnetic compliance), safety, and environmental standards with which the instrument complies.

## Environmental Considerations

This section provides information about the environmental impact of the product.

### Product End-of-Life Handling

Observe the following guidelines when recycling an instrument or component:

**Equipment recycling.** Production of this equipment required the extraction and use of natural resources. The equipment may contain substances that could be harmful to the environment or human health if improperly handled at the product's end of life. To avoid release of such substances into the environment and to reduce the use of natural resources, we encourage you to recycle this product in an appropriate system that will ensure that most of the materials are reused or recycled appropriately.

This symbol indicates that this product complies with the applicable European Union requirements according to Directives 2002/96/EC and 2006/66/EC on waste electrical and electronic equipment (WEEE) and batteries. For information about recycling options, check the Support/Service section of the Tektronix Web site (www.tektronix.com).

### Restriction of Hazardous Substances

This product is classified as Monitoring and Control equipment, and is outside the scope of the 2002/95/EC RoHS Directive.

# Preface

This document provides information on using and servicing the P6450 logic analyzer probe.

## Related Documentation

The following table lists related documentation that is available for your instrument. The documentation is available on the TLA Documentation CD and on the Tektronix Web site (www.Tektronix.com/manuals).

For documentation not specified in the table, contact your local Tektronix representative.

### Table i: Product documentation

| Item | Purpose | Location |
|---|---|---|
| TLA Quick Start User Manual | High-level operational overview | 📖 + 💿 +  www.Tektronix.com |
| Online Help | In depth operation and UI help | ? |
| Installation Quick Reference Cards | High-level installation information | 📖 💿 |
| Installation Manuals | Detailed first-time installation information | 📖 💿 |
| XYZs of Logic Analyzers | Introduction to logic analyzer basics |  www.Tektronix.com |
| Product Specifications | TLA product specification documents | 💿 |
| TPI.NET Documentation | Detailed information for controlling the logic analyzer using .NET | 💿 |
| Field upgrade kits | Upgrade information for your logic analyzer product | 📖 💿 |
| Optional Service Manuals | Self-service documentation for modules and mainframes | 📖 💿 |

## Commonly Used Terms

Refer to the following list of commonly used terms throughout the manual.

| | |
|---|---|
| **cLGA** | An acronym for compression Land Grid Array, a connector that provides an electrical connection between a PCB and the probe input circuitry. |
| **Compression Footprint** | A connectorless, solderless contact between your PCB and the P6450 probes. Connection is obtained by applying pressure between your PCB and the probe through a cLGA c-spring. |
| **D-Max probing technology** | The name that describes the technology used in the P6450 high-density logic analyzer probe. |
| **Flying Lead Set** | A lead set designed to attach to a P6450 probe to provide general-purpose probing capability. (See Figure i.) |

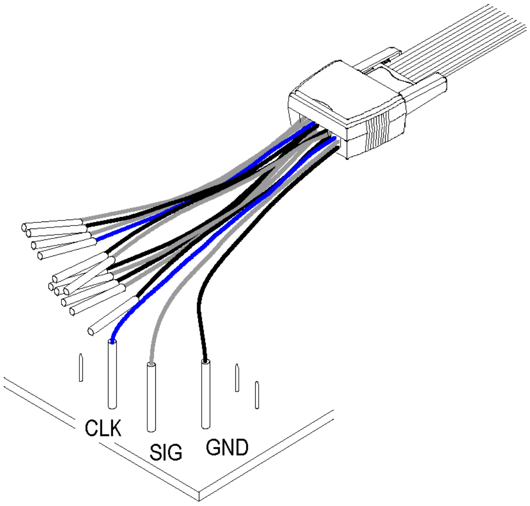

Figure i: Flying lead set

| | |
|---|---|
| **Functional Check Procedure** | Functional check procedures verify the basic functionality of the probes by confirming that the probes recognize signal activity at the probe tips. |
| **Keepout Area** | An area on a printed circuit board in which component, trace, and/or via placement may be restricted. |
| **Module** | The unit that plugs into a mainframe that provides instrument capabilities such as logic analysis. |

| | |
|---|---|
| **Module End** | The end of the probe that plugs into the module unit. |
| **PCB** | An acronym for Printed Circuit Board; also known as Etched Circuit Board (ECB). |
| **Probe** | The device that connects a module with a target system. (See Figure ii.) |

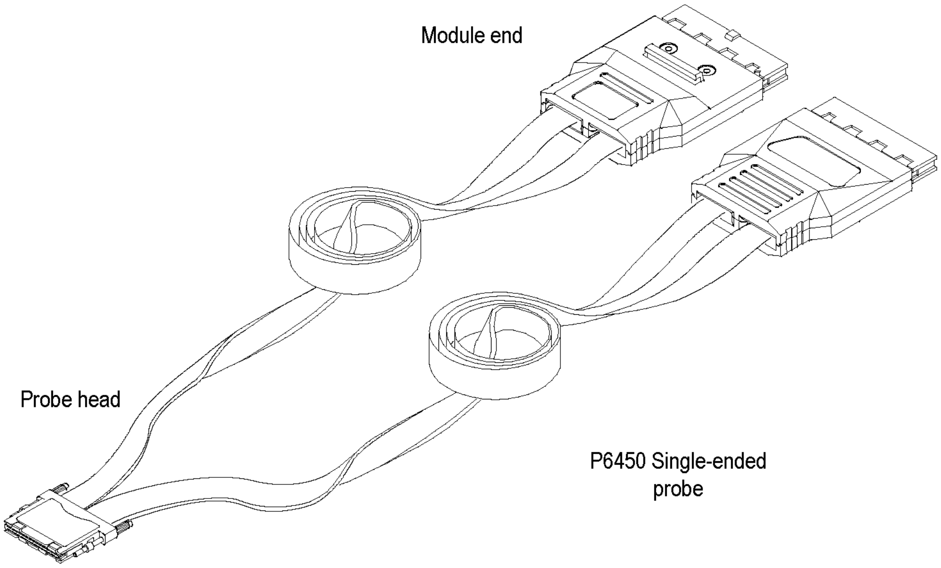

Figure ii: Probe example

| | |
|---|---|
| **Probe Head** | The end of the probe that connects to the target system or probe adapter. |
| **SUT** | An acronym for System Under Test; also referred to as target system. |

# Operating Basics

This section provides a brief description of the Tektronix P6450 High-Density Logic Analyzer Probe, information on attaching color-coded probe labels, and probe and adapter connection instructions from the logic analyzer to the target system.

## Product Description

The P6450 probe is a 34-channel, high-density connectorless probe with D-Max probing technology (See Figure 1.). The probe consists of one probe head that has 34 channels (32 data and 2 clock/qual).

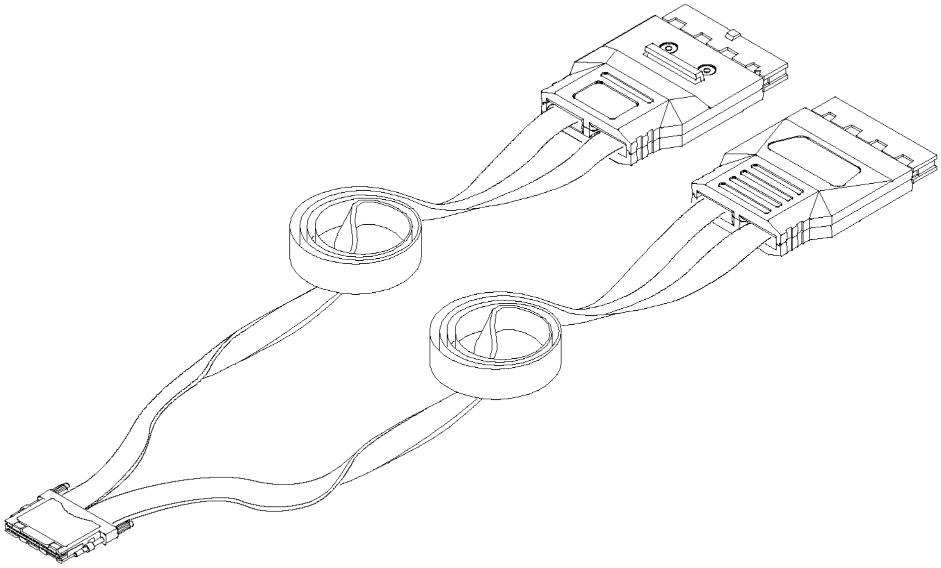

Figure 1: P6450 High-Density probewith D-Max probing technology

The following list details the capabilities and qualities of the P6450 probe:

- Single-ended data inputs
- cLGA contact eliminates need for built-in connector
- Footprint supports direct signal pass-through
- Supports PCB thickness of 1.27 mm to 6.35 mm (0.050 in to 0.250 in)
- Consists of one independent probe head of 34 channels (32 data and 2 clock/quals), and two 34-channel module end connectors.
- Narrow 34-channel probe head makes for easier placement and layout
- 2X mode, (for example, 1:2 demultiplexing) uses one-half of the probe head
- Color-coded keyed attachment

- -3.5 V to +6.5 V input operating range
- 500 mV minimum single-ended signal amplitude
- Minimal loading of 0.7 pF at 20 kΩ to ground
- Operation in normal or inverted polarity is acceptable (clock only)

## Attaching Probe Labels

When you purchase the P6450 logic analyzer probe, you must apply the color-coded labels as described in this section. The labels help you identify the probe connections at the logic analyzer end and at the target system end.

The following table lists the probe section and label color combinations. (See Table 1.) Refer to the table and to the following figure when you attach the probe labels. (See Figure 2 on page 4.)

Table 1: Probe section and label combinations

| Probe section | Channels | Label color | Probe section | Channels | Label color |
|---|---|---|---|---|---|
| A3-A2 | CK0,<br>A3:7-0,<br>A2:7-0 | Brown | A1-A0 | CK1,<br>A1:7-0,<br>A0:7-0 | Orange |
| D3-D2 | QUAL0,<br>D3:7-0,<br>D2:7-0 | Blue | D1-D0 | CK2,<br>D1:7-0,<br>D0:7-0 | Yellow |
| C3-C2 | CK3,<br>C3:7-0,<br>C2:7-0 | White | C1-C0 | QUAL1,<br>C1:7-0,<br>C0:7-0 | Gray |
| E3-E2 | QUAL3,<br>E3:7-0,<br>E2:7-0 | Green | E1-E0 | QUAL2,<br>E1:7-0,<br>E0:7-0 | Violet |

### P6450 Labels

Use the following instructions to attach probe labels to your Tektronix P6450 Logic Analyzer Probe.

**NOTE.** *Always use flat-nosed tweezers to remove the labels from the sheet of labels. Never peel labels with your fingers. The labels are made of soft vinyl and can stretch and distort easily. To avoid stretching the label, always grasp it from the top right corner while removing it from the sheet of labels.*

*The adhesive on the vinyl labels is extremely strong. Carefully align each label to the intended outline on the module end and probe head before attaching it to the probe. Once labels are placed on the probe, they become very difficult to remove.*

You will be attaching labels to the logic analyzer end and both sides of the probe head. Use the following steps to attach the probe labels:

1. Identify the module end of the probe cable. (See Figure 2 on page 4.)
2. From the sheet of labels, locate the color-coded label for the logic analyzer end of the probe cable.
3. Attach the matching colored labels to the probe head on the other end of the probe cable. (See Figure 2 on page 4.)

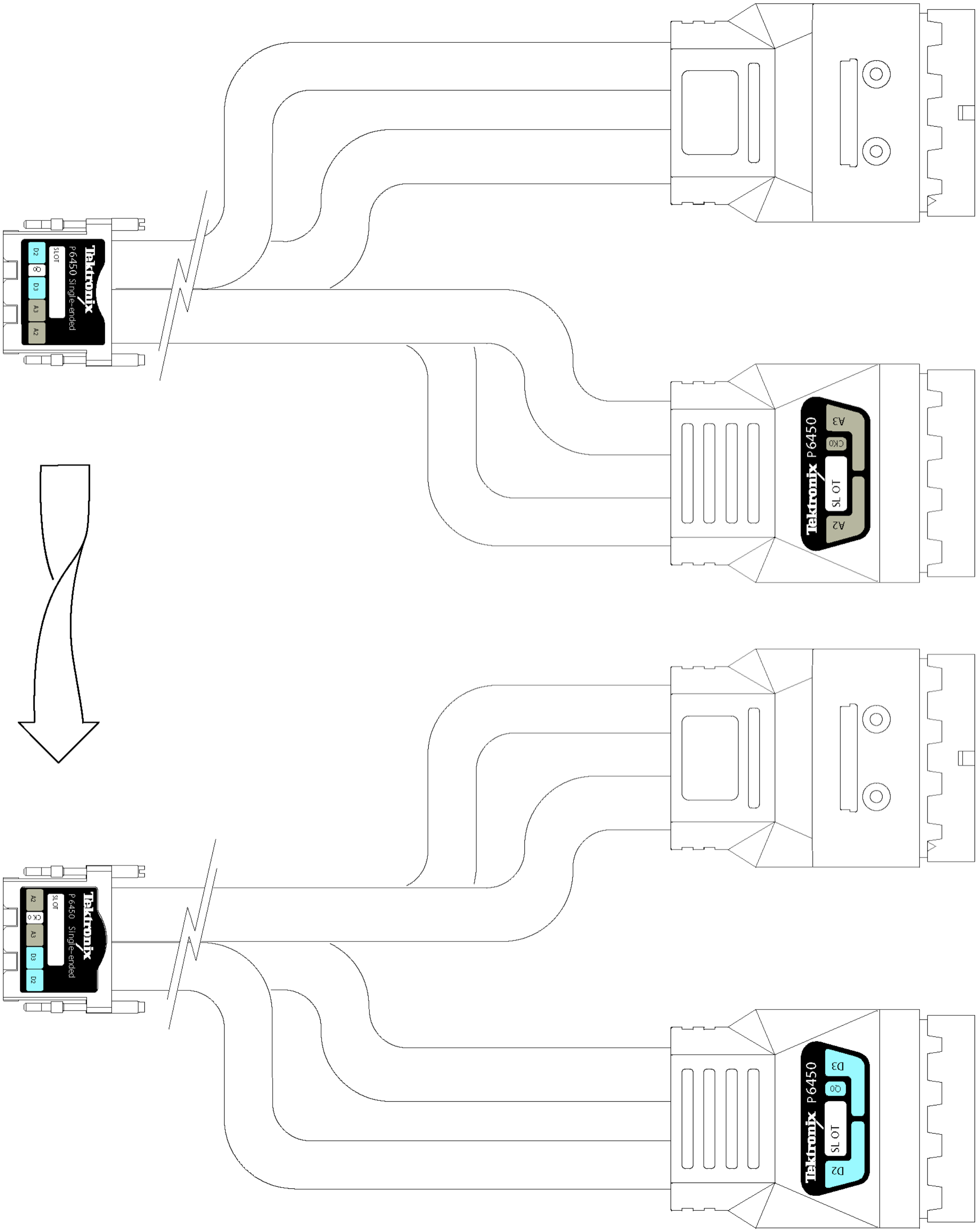

**Figure 2: Attaching labels to the P6450 probe**

## Connecting the Probes to the Logic Analyzer

Connect the logic analyzer probe and the optional retaining brackets as shown. (See Figure 3.) The retaining brackets and hardware ship with the logic analyzer.

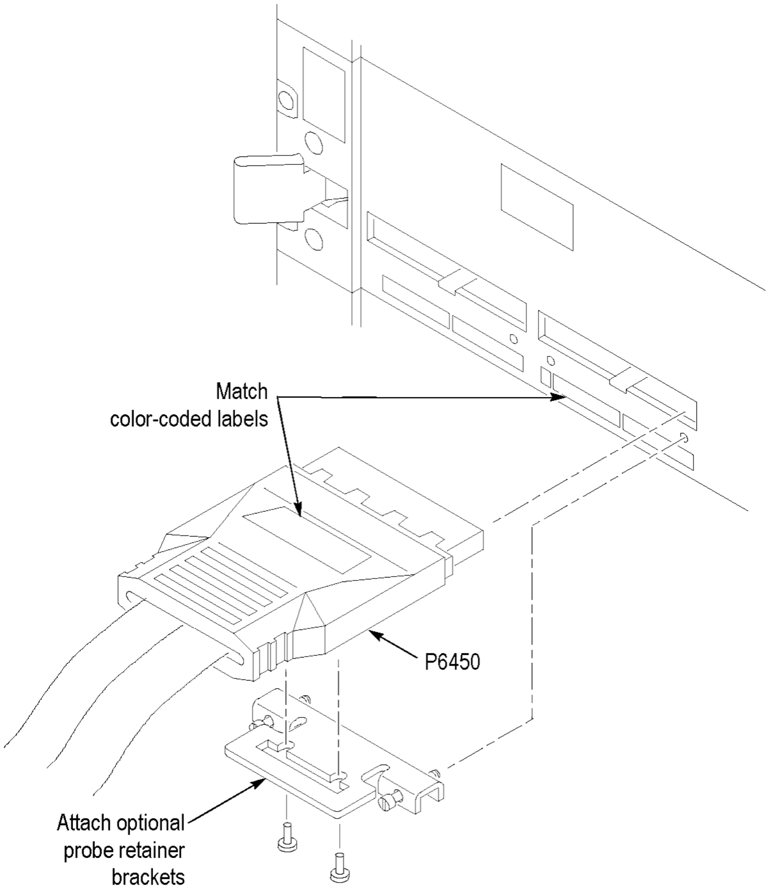

Figure 3: Connecting the logic analyzer probe

**NOTE.** *The probe can be connected to the logic analyzer when it is powered on.*

## Connecting the Probes to the Target System

You can connect the P6450 probe to the target system without turning off the power to the target system. The target system must have the probe retention assembly installed. Installation procedures are described on the following pages.

### Cleaning the Compression Footprints

The following procedure is recommended to obtain best performance.

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⚠ ***CAUTION.*** *To avoid electrical damage, always power off your target system before cleaning the compression footprint.*

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Prior to connecting the probe to the target system, the compression footprints on the board should be properly cleaned, according to the following steps:

1. Use a lint-free, clean-room cloth lightly moistened with electronic/reagent grade isopropyl alcohol, and gently wipe the footprint surface.
2. Remove any remaining lint using a nitrogen air gun or clean, oil-free dry air.

### Using the Probe Retention Assembly

The probe retention assembly provides a housing around the connector footprint to help stabilize the probe. To install the probe retention assembly on the circuit board, do the following:

1. Locate the correct footprint. If you intend to use multiple probes, your PCB has multiple footprints. Be careful to select the correct one.
2. Clean the compression footprint as described above.
3. Align the retention assembly over the footprint so that the keying pin on the retention assembly lines up with the keying pin hole on the footprint. (See Figure 4 on page 7.)
4. Insert the retention assembly into the holes in the footprint on the PCB.

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***NOTE.*** *The following two steps are important to ensure that the retention assembly is correctly mounted and that the probe makes proper contact with the PCB.*

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5. Hold the retention assembly so that it is firmly flush with the surface of the footprint, and the four anchoring posts extend through the circuit board to the opposite side.
6. Using a pair of needle-nose pliers, grasp one of the posts. Using the circuit board hole as a fulcrum, bend the post outward so that it is flush with the PCB

surface, anchoring the assembly to the PCB. Bend the other three posts in the same manner. (See Figure 4 on page 7.)

7. Solder the anchoring posts to the PCB. (See Figure 4 on page 7.)

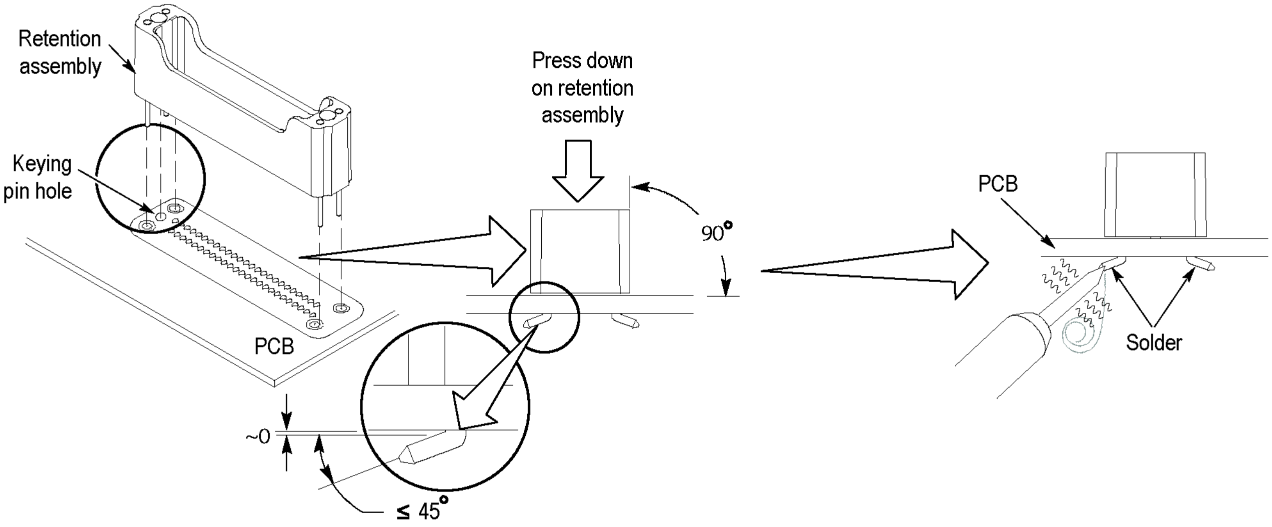


**Figure 4: Installing the probe retention assembly**

### Handling the cLGA Interface Clip (Probe Head)

The cLGA interface clip in the probe head should always be handled with care. Keep the following points in mind when you handle the clip:

- Always handle the cLGA interface clip by the outer edges, and be careful to avoid the contacts in the center. Do not touch the contacts with your fingers, tools, wipes, or any other devices. (See Figure 5.)

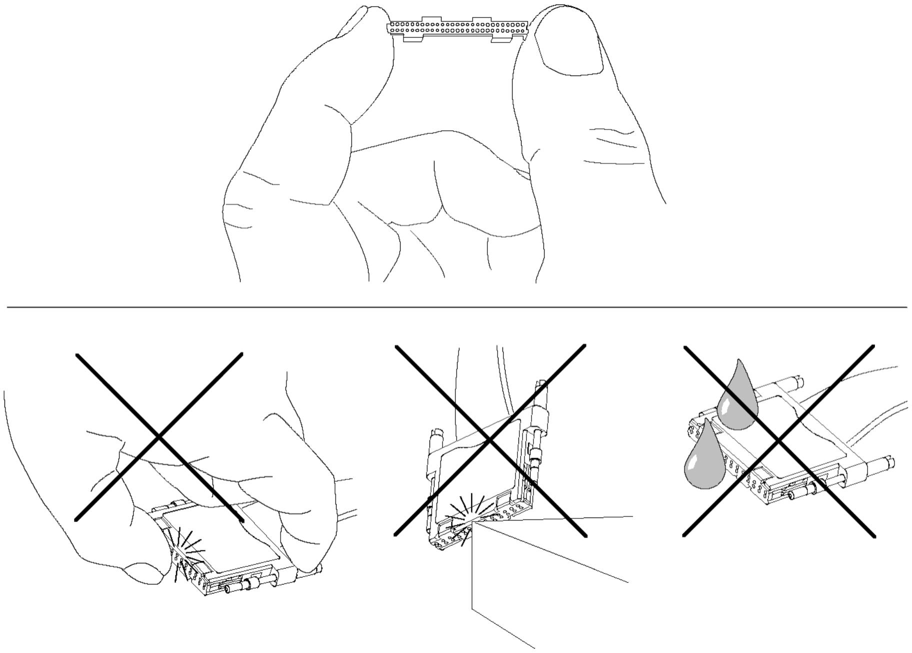


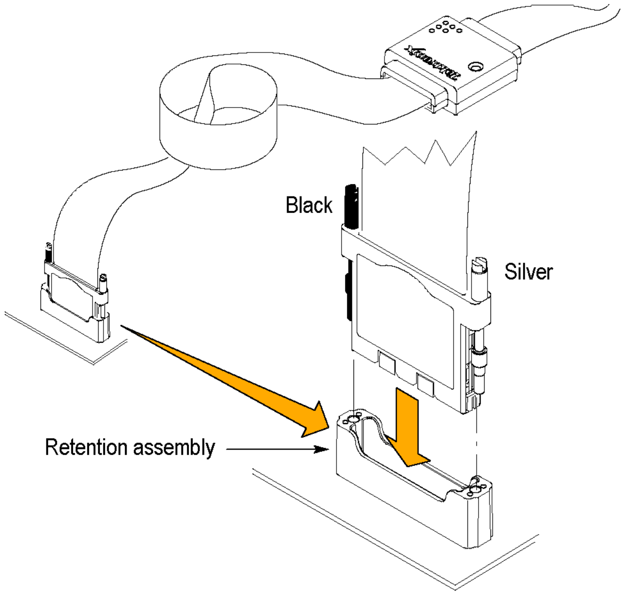
Figure 5: Proper handling of the interface clip

- Do not expose the connector to liquids or dry chemicals.
- If the board pad array needs to be cleaned, only use isopropyl alcohol and lint-free cloth as described above.
- Immediately following cleaning, or immediately prior to placement of connector to circuit board, blow off the board pad array and connector contact array with clean, oil-free dry air or nitrogen to remove loose debris. First start the blowing process by aiming away from the array areas, and then sweep across the pad and contact arrays in a repeated motion to remove loose debris.
- Place the connector onto the board pad array using the bosses or locator pins for alignment. Use care to prevent incidental contact with other surfaces or edges in the connector contact array area prior to board placement.
- Always store the probe head in the protective cover when not in use. (See Figure 8 on page 12.)

## Connect the Probe

Connect the probes using the following steps. (See Figure 6.)

1. Align the silver screw on the probe to the silver side of the retention assembly.



Note: The retention assembly is visually keyed (one side is black and one side is silver).

**Figure 6: Connecting the probes to the target system**

2. Start both screws in the retention assembly, and tighten them evenly to ensure that the probe approaches and mates squarely to the PCB. If access is limited, use the adjustment tool that came with your probe. The probe is completely fastened to the PCB when the screws stop in the assembly.
3. Verify that all of the channels are functional.

## Troubleshooting Probe Connections to the SUT

The most obvious symptom of a problem with the probe installation is seeing incorrect data in the logic analyzer acquisition. However, the nature of the incorrect data has a very consistent characteristic; the data from multiple channels go to a logic low and stay there. Intermittent bad data, or a single dead channel are not failures typically associated with probe installation problems.

1. Slightly move the probe head to either side, or press down on the probe head while making new acquisitions. If good data is now being acquired, then the probe mounting is most likely the cause.
2. If good data is not acquired, then remove the probe and check the retention assembly for too much play. If there is significant play, then the probe mounting is most likely the cause.

3. If the retention assembly has minimal play and you cannot see a gap between the bottom of the assembly and the circuit board surface, then move the probe with bad data from one logic analyzer probe location to another.

4. If the problem follows the probe, then the probe is the problem. Visually inspect the cLGA interface clip on the probe for any damage or missing c-spring metal contacts.

   If there is damage to the interface clip, or if any c-spring metal contacts are missing, replace the cLGA interface clip. (See page 27, *Replacing the cLGA Clip*.)

5. If the problem doesn't follow the probe, it is either the logic analyzer or the probe connection at its previous location. Move the probe back to the original location to be certain it was not a connection problem at the logic analyzer end.

6. Place another probe in the retention assembly of the original probe. If the new probe acquires data, then the old probe is probably at fault.

## Dressing the Probe Cables

Use the Velcro cable managers to combine the cables together or to help relieve strain on the probe connections.

Hang the probe cables so that you relieve the tension on the probes at the retention posts. (See Figure 7.)

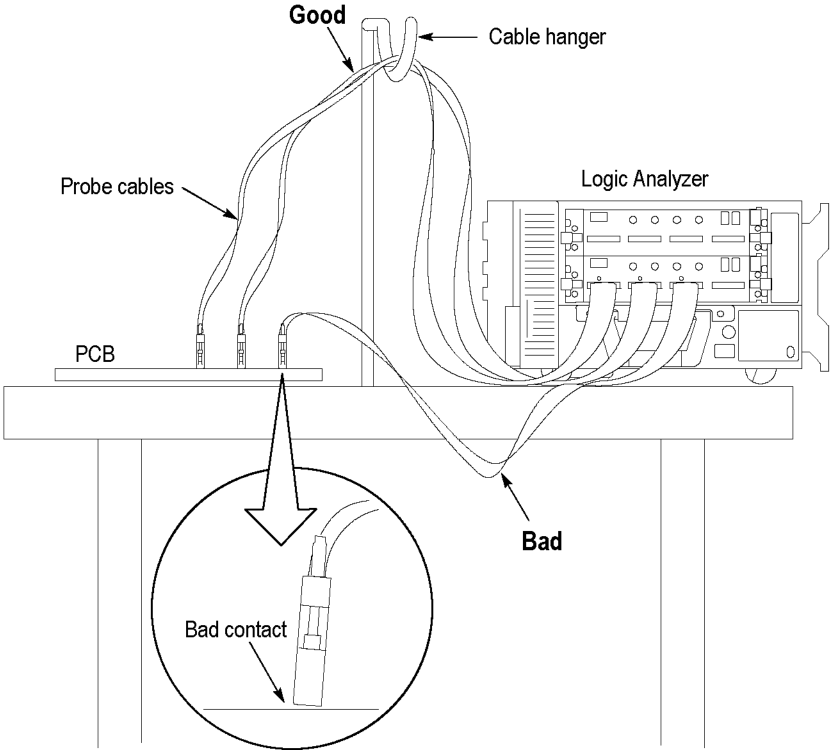


Figure 7: Proper dressing of the probe cables

## Storing the Probe Head

To protect the interface clip, it is important to properly store the probe head when the probe is not in use. (See Figure 8.)

Gently slide the probe cover over the probe end and store the probe.

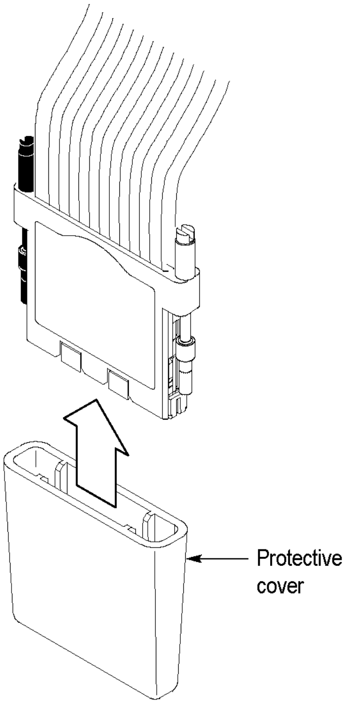


Figure 8: Protecting the probe head

# Reference

This section provides reference information for the P6450 High-Density Probe with D-Max probing technology.

## Designing an Interface Between the Probes and a Target System

Once you have determined which probe is required, use the following information to design the appropriate connector into your target system board.

### Signal Fixturing Considerations

This section contains information to consider for signal fixturing.

**Clocks and Qualifiers.** Every logic analyzer has some special purpose input channels. Inputs designated as clocks can cause the logic analyzer to store data. Qualifiers Clocks Every logic analyzer has some special purpose input channels. Inputs designated as clocks can cause the logic analyzer to store data. Qualifier channels can be logically ANDed and ORed with clocks to further define when the logic analyzer should latch data from the system under test. Routing the appropriate signals from your design to these inputs ensures that the logic analyzer can acquire data correctly. Unused clocks can be used as qualifier signals.

Depending on the channel width, each TLA5000B Series logic analyzer will have a different set of clock and qualifier channels. The following table shows the clock and qualifier channels available for each module.

Table 2: Logic analyzer clock and qualifier availability

| TLA Module | Clock Inputs | | | | Qualifier Inputs | | | |
|---|---|---|---|---|---|---|---|---|
| | CLK:0 | CLK:1 | CLK:2 | CLK:3 | QUAL:0 | QUAL:1 | QUAL:2 | QUAL:3 |
| TLA5201B | × | | | × | | | | |
| TLA5202B | × | × | × | × | | | | |
| TLA5203B | × | × | × | × | × | × | | |
| TLA5204B | × | × | × | × | × | × | × | × |

All clock and qualifier channels are stored. The logic analyzer always stores the logic state of these channels every time it latches data.

Since clock and qualifier channels are stored in the logic analyzer memory, there is no need to double probe these signals for timing analysis. When switching from state to timing analysis, all of the clock and qualifier signals will be visible. This allows you to route signals not needed for clocking to the unused clock and qualifier channels.

It is a good practice to take advantage of the unused clock and qualifier channels to increase your options for when you will latch data. Routing several clocks and strobes in your design to the logic analyzer clock inputs will provide you with a greater flexibility in the logic analyzer Setup menu.

As an example, look at a microprocessor with a master clock, data strobe, and an address strobe. Routing all three of these signals to logic analyzer clock inputs will enable you to latch data on the processor master clock, only when data is strobed, or only when address is strobed. Some forethought in signal routing can greatly expand the ways in which you can latch and analyze data.

A microprocessor also provides a good example of signals that can be useful as qualifiers. There are often signals that indicate data reads versus data writes (R/W), signals that show when alternate bus masters have control of the processor buses (DMA), and signals that show when various memory devices are being used (ChipSel). All of these signals are good candidates for assignment to qualifier channels.

By logically ANDing the clock with one of these qualifiers you can program the logic analyzer to store only data reads or data writes. Using the DMA signal as a qualifier provides a means of filtering out alternate bus master cycles. Chip selects can limit data latching to specific memory banks, I/O ports, or peripheral devices.

**Demultiplexing Multiplexed Buses.** TLA5000B Series logic analyzers support 2X demultiplexing. Each signal on a dual multiplexed bus can be demultiplexed into its own logic analyzer channel. See the following table to determine the correct channel groups to use.

Table 3: 2X Demultiplexing source-to-destination channel assignments

| Source connecting channel groups | Destination channels receiving target system test data | | | |
|---|---|---|---|---|
| | TLA5204B | TLA5203B | TLA5202B | TLA5201B |
| A3:7-0 | D3:7-0 | D3:7-0 | C3:7-0 | C3:7-0 |
| A2:7-0 | D2:7-0 | D2:7-0 | C2:7-0 | C2:7-0 |
| A1:7-0 | D1:7-0 | D1:7-0 | D1:7-0 | |
| A0:7-0 | D0:7-0 | D0:7-0 | D0:7-0 | |
| C3:7-0 | C1:7-0 | C1:7-0 | | |
| C2:7-0 | C0:7-0 | C0:7-0 | | |
| E3:7-0 | E1:7-0 | | | |
| E2:7-0 | E0:7-0 | | | |
| CLK:0 | QUAL:1 | QUAL:1 | | |
| CLK:1 | QUAL:0 | QUAL:0 | | |
| CLK:2 | QUAL:3 | | | |
| CLK:3 | QUAL:2 | | | |

When demultiplexing data there is no need to connect the destination channels to the multiplexed bus. Data from the source channels are routed to the destination channels internal to the logic analyzer. The table 3 shows the mapping of source channels to destination channels. (See Table 3 on page 14.)

Demultiplexing affects only the main memory for the destination channels. This means that the MagniVu memory is filled with data from whatever is connected to the demultiplexing destination channel probe inputs. This provides an opportunity to acquire high resolution MagniVu data on a few extra channels. Connecting the demultiplexing destination channels to other signals will allow viewing of their activity in the MagniVu memory but not the main memory.

**High Resolution Timing.** The high resolution timing mode provides double the normal 500 MHz sample rate on one-half of the channels. By trading half of the analyzer's channels, the remaining channels can be sampled at a 1 GHz rate with double the memory depth.

By taking care to assign critical signals to the demultiplexing source channels, you can obtain extra timing resolution where it is most needed. Since demultiplexing affects only the main memory you will still have the MagniVu data available for all of the signals that are disconnected from the main memory when you switch to the high resolution timing modes.

**Range recognition .** When using range recognizers, the probe groups and probe channels must be in hardware order. Probe groups must be used from the most-significant probe group to the least-significant probe group based on the following order:

C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0

Probe channels must be from the most-significant channel to the least-significant channel based on the following order:

7 6 5 4 3 2 1 0

The above examples assumes a 136-channel logic analyzer. The missing channels in logic analyzers with fewer than 136 channels are ignored.

# Board Design

This section provides information that helps you design your PCB mechanically and electrically for use with the P6450 probe.

## Probe Dimensions

The following figure shows the dimensions for the P6450 probe. (See Figure 9.)

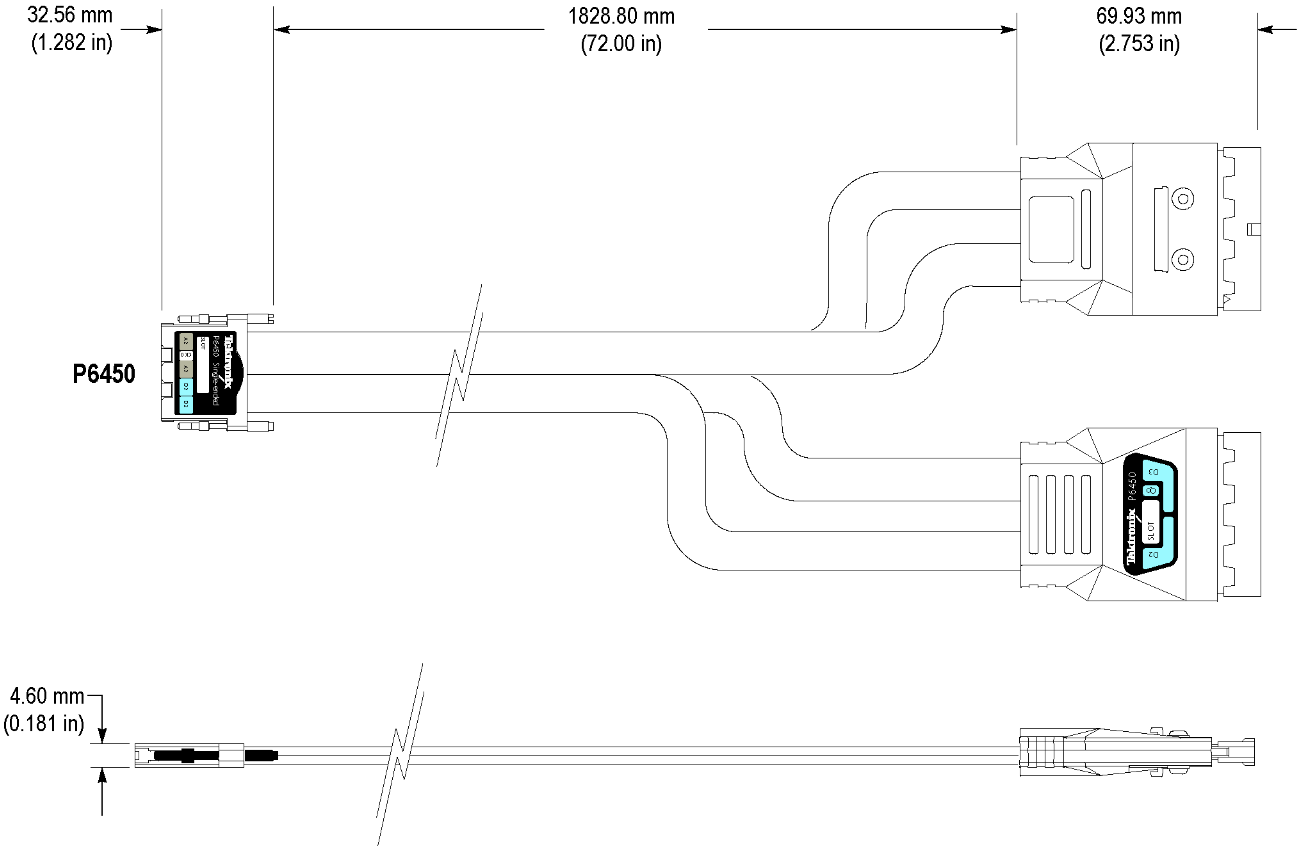


Figure 9: P6450 probe dimensions

## Probe Retention Assembly Dimensions and Keepout

The probe retention assembly provides a housing around the connector footprint to help stabilize the probe.

All dimensions are per standard IPC tolerance, which is ±0.004 in. (See Figure 10.)

**CAUTION.** *To avoid solder creep, bend the assembly wires out after you insert the wires in the board, and then solder the wires.*

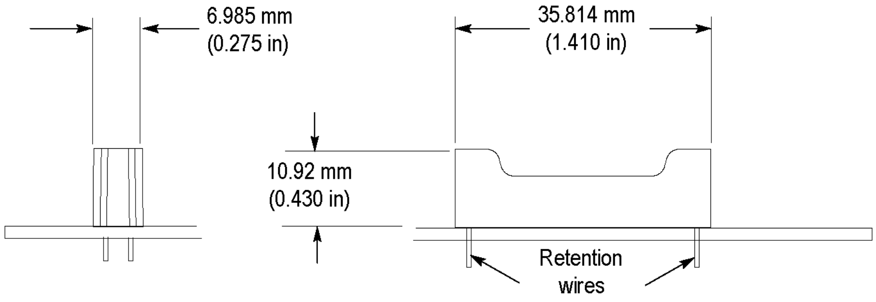


**Figure 10: Alternate retention assembly dimensions**

The following figure shows the keep out area required for the alternate retention assembly. (See Figure 11.)

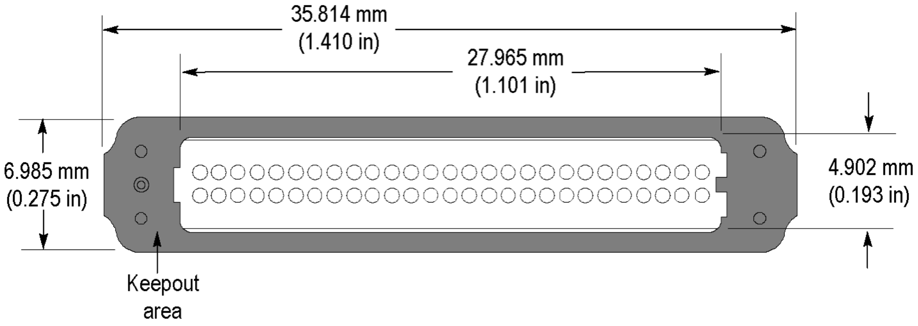


**Figure 11: Keepout area**

### Side-by-side and End-to-end Layout Dimensions

The following figure shows the dimensions for side-by-side footprint layout. (See Figure 12.)

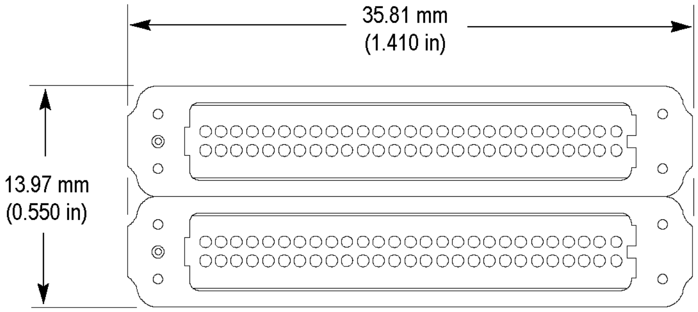


Figure 12: Side-by-side layout

The following figure shows the dimensions for an end-to-end footprint layout. (See Figure 13.)

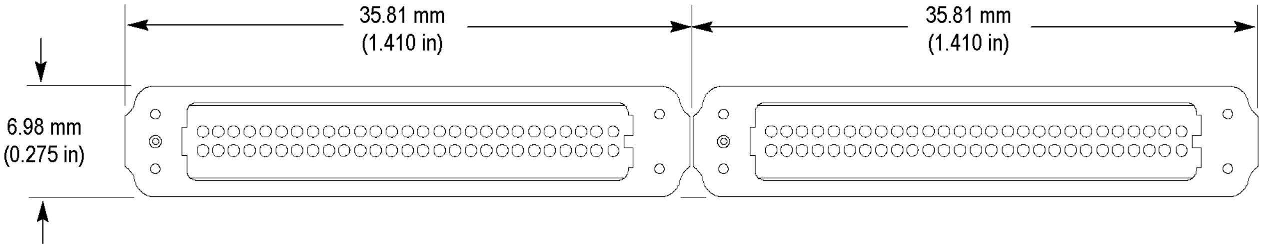


Figure 13: End-to-end layout

## Signal Routing

The following figure shows examples of pass-through signal routing for a single-ended data configuration. (See Figure 14.)

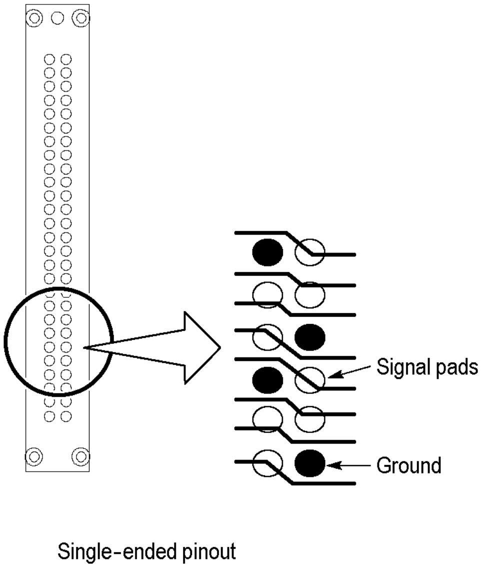


**Figure 14: Signal routing on the target system**

## Mechanical Considerations

This section provides information on compression footprint requirements and physical attachment requirements.

The PCB holes, in general, do not have an impact upon the integrity of your signals when the signals routed around the holes have the corresponding return current plane immediately below the signal trace for the entire signal path from driver to receiver.

---

***NOTE.*** *For optimum signal integrity, there should be a continuous, uninterrupted ground return plane along the entire signal path.*

---

## Electrical Considerations

This section provides information on transmission lines and load models for the P6450 probe.

The low-frequency model is typically adequate for rise and fall times of 1 ns or slower in a typical 25 Ω source impedance environment (50 W runs with a pass-through connection). For source impedance outside this range, and/or rise and fall times faster than 1 ns, use the high-frequency model to determine if a significant difference is obtained in the modeling result.

The compression land pattern pad is not part of the load model. Make sure that you include the compression land pad in the modeling.

**Transmission Lines.** Due to the high performance nature of the interconnect, ensure that stubs, which are greater than 1/4 length of the signal rise time, are modeled as transmission lines.

**P6450 Probe Load Model.** The following electrical model includes a low-frequency model of the High-Density Single-Ended Probe. (See Figure 15.)

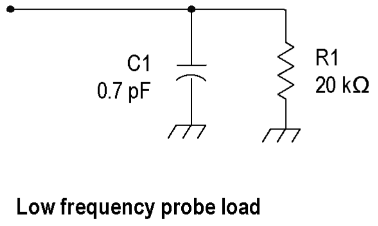


Figure 15: High-Density probe load model

## Probe Footprint Dimensions

Use the probe footprint dimensions to lay out your circuit board pads and holes for attaching the retention posts. (See Figure 16 on page 21.) If you are using the alternate retention assembly, all dimensions remain the same as shown below, except the overall length and width. (See Figure 10 on page 17.) Pad finishes that are supported include immersion gold, immersion silver, and hot air solder level.

All dimensions are per standard IPC tolerance, which is ±0.004 in.

---

***NOTE.*** *Tektronix recommends using immersion gold surface finish for best performance.*

*Tektronix also recommends that the probe attachment holes float or remain unconnected to a ground plane. This prevents overheating the ground plane and promotes quicker soldering of the retention posts to your PCB. The probe retention posts are designed to allow you to solder the retention posts from either side of your PCB.*

---

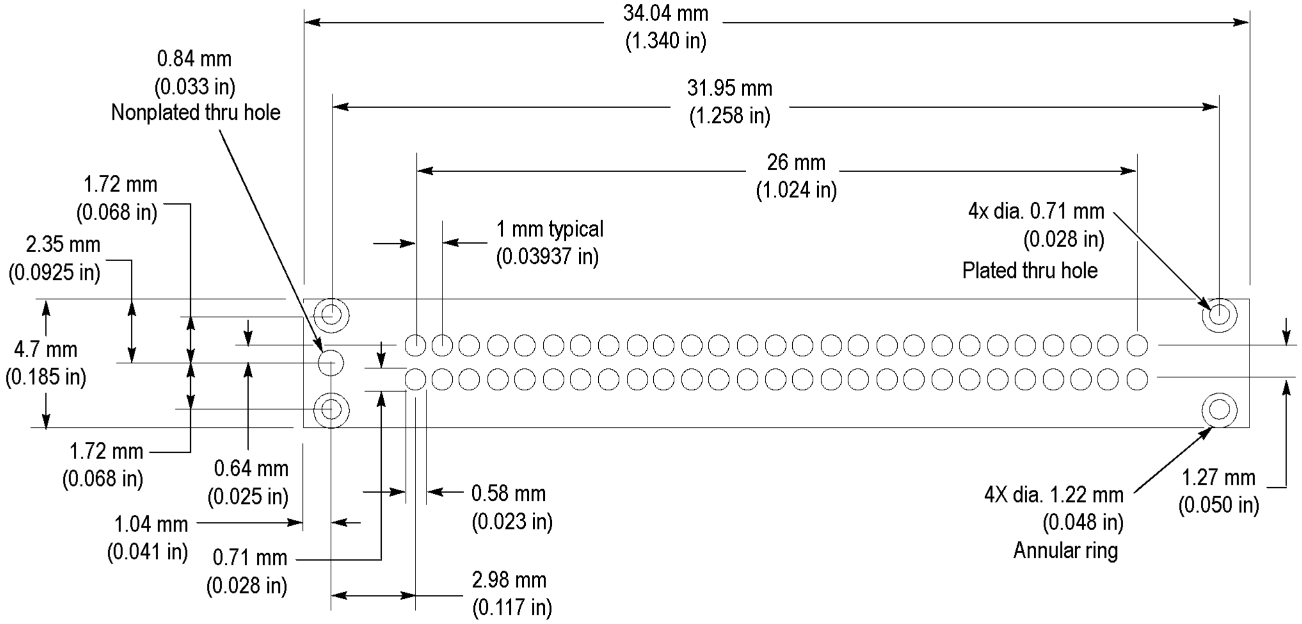


**Figure 16: Probe footprint dimensions on the PCB**

***NOTE.*** *You must maintain a solder mask web between the pads when traces are routed between pads on the same layer. The solder mask must not encroach onto the pads within the pad dimensions. (See Figure 11 on page 17.)*

## Other Design Considerations

### Via-in-pad

Traditional layout techniques require vias to be located next to a pad and a signal routed to the pad, causing a stub and more PCB board area to be used for the connection. Many new digital designs require you to minimize the electrical effects of the logic analyzer probing that you design into the circuit board.

Using via-in-pad to route signals to the pads on the circuit board allows you to minimize the stub length of the signals on your board, thus providing the smallest intrusion to your signals. It also enables you to minimize the board area that is used for the probe footprint and maintain the best electrical performance of your design.

The following figure shows a footprint example where two pads use vias. (See Figure 17.). Detail A describes the recommended position of the via with respect to the pad.

All dimensions are per standard IPC tolerance, which is ±0.004 in.

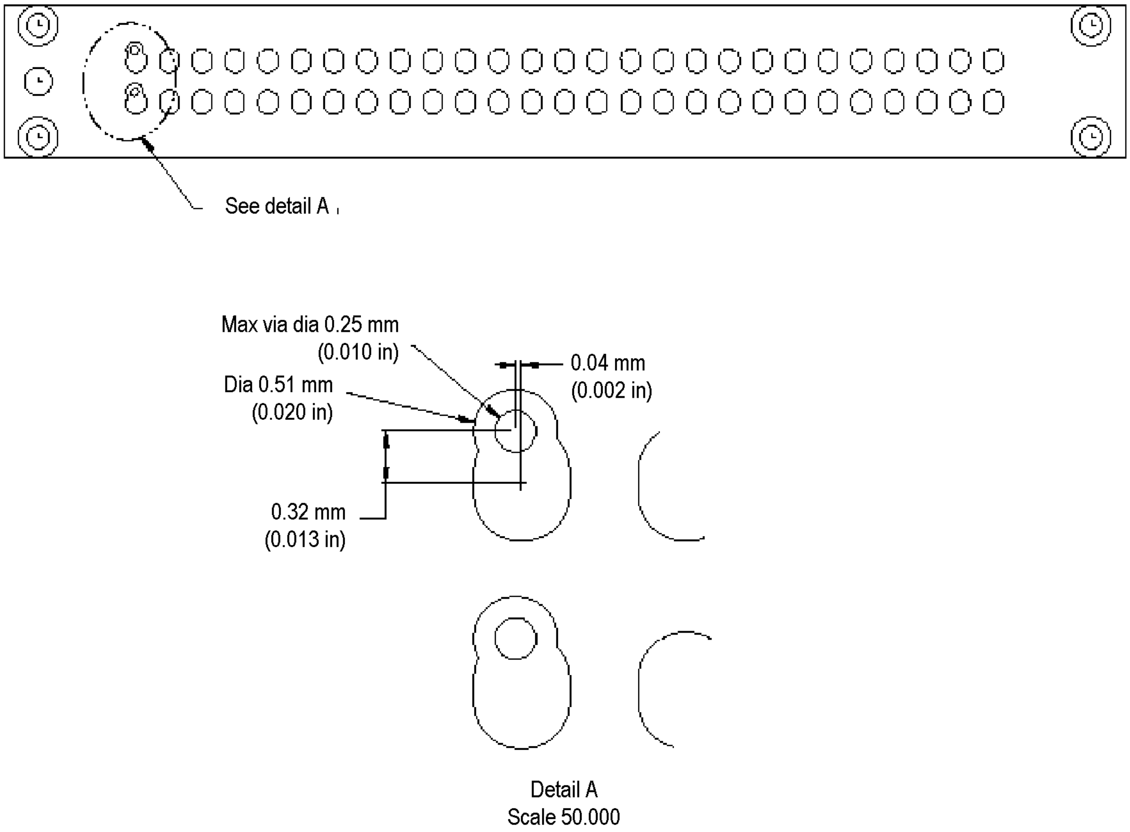


Figure 17: Optional Via-in-Pad placement recommendation

## Probe Pinout Definition and Channel Assignment

This section contains probe pinout definitions and channel assignment tables for the P6450 probe.

### P6450 Single-ended Probewith D-Max probing technology

The following figure shows the pad assignments, pad numbers, and signal names for the PCB footprint of the P6450 single-ended logic analyzer probe. (See Figure 18.) The P6450 probe has 32 data channels, one clock, and one qualifier for each footprint.

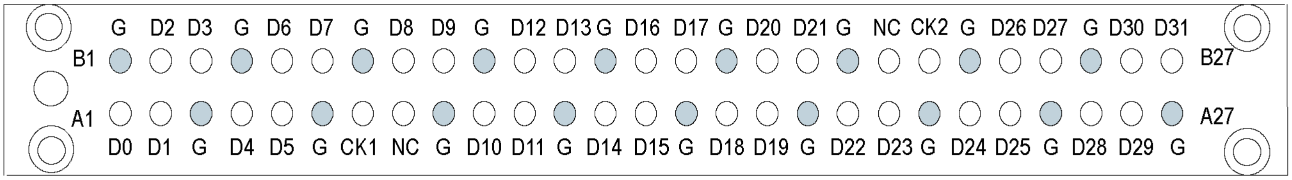


**Figure 18: P6450 single-ended PCB footprint pinout detail**

The following table lists the channel mapping to a logic analyzer module for a P6450 single-ended logic analyzer probe. (See Table 4.)

**Table 4: Channel assignment for a P6450 single-ended logic analyzer probe**

| Number of channels | | 136 | 136 or 102 | 136 or 102 | 136 or 102 | 68 | 68 or 34 |
|---|---|---|---|---|---|---|---|
| **Pin** | **Signal** | **Probe4** | **Probe 3** | **Probe 2** | **Probe 1** | **Probe 2** | **Probe 1** |
| A1 | D0 | E2:0 | A2:0 | A0:0 | C2:0 | A0:0 | C2:0 |
| A2 | D1 | E2:1 | A2:1 | A0:1 | C2:1 | A0:1 | C2:1 |
| A3 | GND | GND | GND | GND | GND | GND | GND |
| A4 | D4 | E2:4 | A2:4 | A0:4 | C2:4 | A0:4 | C2:4 |
| A5 | D5 | E2:5 | A2:5 | A0:5 | C2:5 | A0:5 | C2:5 |
| A6 | GND | GND | GND | GND | GND | GND | GND |
| A7 | CK1 | Q3 | CK0 | CK1 | CK3 | CK1 | CK3 |
| A8 | NC | NC | NC | NC | NC | NC | NC |
| A9 | GND | GND | GND | GND | GND | GND | GND |
| A10 | D10 | E3:2 | A3:2 | A1:2 | C3:2 | A1:2 | C3:2 |
| A11 | D11 | E3:3 | A3:3 | A1:3 | C3:3 | A1:3 | C3:3 |
| A12 | GND | GND | GND | GND | GND | GND | GND |
| A13 | D14 | E3:6 | A3:6 | A1:6 | C3:6 | A1:6 | C3:6 |
| A14 | D15 | E3:7 | A3:7 | A1:7 | C3:7 | A1:7 | C3:7 |
| A15 | GND | GND | GND | GND | GND | GND | GND |
| A16 | D18 | E1:5 | D3:5 | D1:5 | C1:5 | D1:5 | A3:5 |
| A17 | D19 | E1:4 | D3:4 | D1:4 | C1:4 | D1:4 | A3:4 |
| A18 | GND | GND | GND | GND | GND | GND | GND |
| A19 | D22 | E1:1 | D3:1 | D1:1 | C1:1 | D1:1 | A3:1 |

**Table 4: Channel assignment for a P6450 single-ended logic analyzer probe (cont.)**

| Number of channels | | 136 | 136 or 102 | 136 or 102 | 136 or 102 | 68 | 68 or 34 |
|---|---|---|---|---|---|---|---|
| **Pin** | **Signal** | **Probe4** | **Probe 3** | **Probe 2** | **Probe 1** | **Probe 2** | **Probe 1** |
| A20 | D23 | E1:0 | D3:0 | D1:0 | C1:0 | D1:0 | A3:0 |
| A21 | GND | GND | GND | GND | GND | GND | GND |
| A22 | D24 | E0:7 | D2:7 | D0:7 | C0:7 | D0:7 | A2:7 |
| A23 | D25 | E0:6 | D2:6 | D0:6 | C0:6 | D0:6 | A2:6 |
| A24 | GND | GND | GND | GND | GND | GND | GND |
| A25 | D28 | E0:3 | D2:3 | D0:3 | C0:3 | D0:3 | A2:3 |
| A26 | D29 | E0:2 | D2:2 | D0:2 | C0:2 | D0:2 | A2:2 |
| A27 | GND | GND | GND | GND | GND | GND | GND |
| B1 | GND | GND | GND | GND | GND | GND | GND |
| B2 | D2 | E2:2 | A2:2 | A0:2 | C2:2 | A0:2 | C2:2 |
| B3 | D3 | E2:3 | A2:3 | A0:3 | C2:3 | A0:3 | C2:3 |
| B4 | GND | GND | GND | GND | GND | GND | GND |
| B5 | D6 | E2:6 | A2:6 | A0:6 | C2:6 | A0:6 | C2:6 |
| B6 | D7 | E2:7 | A2:7 | A0:7 | C2:7 | A0:7 | C2:7 |
| B7 | GND | GND | GND | GND | GND | GND | GND |
| B8 | D8 | E3:0 | A3:0 | A1:0 | C3:0 | A1:0 | C3:0 |
| B9 | D9 | E3:1 | A3:1 | A1:1 | C3:1 | A1:1 | C3:1 |
| B10 | GND | GND | GND | GND | GND | GND | GND |
| B11 | D12 | E3:4 | A3:4 | A1:4 | C3:4 | A1:4 | C3:4 |
| B12 | D13 | E3:5 | A3:5 | A1:5 | C3:5 | A1:5 | C3:5 |
| B13 | GND | GND | GND | GND | GND | GND | GND |
| B14 | D16 | E1:7 | D3:7 | D1:7 | C1:7 | D1:7 | A3:7 |
| B15 | D17 | E1:6 | D3:6 | D1:6 | C1:6 | D1:6 | A3:6 |
| B16 | GND | GND | GND | GND | GND | GND | GND |
| B17 | D20 | E1:3 | D3:3 | D1:3 | C1:3 | D1:3 | A3:3 |
| B18 | D21 | E1:2 | D3:2 | D1:2 | C1:2 | D1:2 | A3:2 |
| B19 | GND | GND | GND | GND | GND | GND | GND |
| B20 | NC | NC | NC | NC | NC | NC | NC |
| B21 | CK2 | Q2 | Q0 | CK2 | Q1 | CK2 | CK0 |
| B22 | GND | GND | GND | GND | GND | GND | GND |
| B23 | D26 | E0:5 | D2:5 | D0:5 | C0:5 | D0:5 | A2:5 |
| B24 | D27 | E0:4 | D2:4 | D0:4 | C0:4 | D0:4 | A2:4 |
| B25 | GND | GND | GND | GND | GND | GND | GND |
| B26 | D30 | E0:1 | D2:1 | D0:1 | C0:1 | D0:1 | A2:1 |
| B27 | D31 | E0:0 | D2:0 | D0:0 | C0:0 | D0:0 | A2:0 |

# Specifications

## Mechanical and Electrical Specifications

The mechanical and electrical specifications for the P6450 probe are listed below. (See Table 5.) The electrical specifications apply when the probe is connected between a compatible logic analyzer and a target system.

Refer to the *Tektronix TLA5000B Logic Analyzer Product Specifications & Performance Verification* document (available on the *Tektronix Logic Analyzer Family Product Documentation* CD or downloadable from the Tektronix Web site) for a complete list of specifications, including overall system specifications.

**Table 5: Mechanical and electrical specifications**

| Characteristic | P6450 |
|---|---|
| Threshold accuracy | ±100 mV |
| Input resistance | 20 kΩ ±1% |
| Input capacitance | 0.7 pF |
| Minimum digital signal swing | 500 mV p-p |
| Maximum nondestructive input signal to probe | ±15 V |
| Delay from probe tip to module input connector | 7.33 ns |
| Probe length | 1.8 m (6 ft) |
| Operating range | +6.5 V to -3.5 V |

The following table lists environmental specifications for the probe. (See Table 6.) The probe is designed to meet Tektronix standard 062-2847-00 class 5.

**Table 6: Environmental specifications**

| Characteristic | P69xx |
|---|---|
| Temperature<br>Operating<br>Non-operating | 0 °C to +50 °C (0 °F to +122 °F)<br>-51 °C to +71 °C (-60 °F to +160 °F) |
| Humidity | 10 °C to 30 °C (+50 °F to +86 °F) 95% relative humidity<br>30 °C to 40 °C (+86 °F to +104 °F) 75% relative humidity<br>40 °C to 50 °C (+104 °F to +122 °F) 45% relative humidity |
| Altitude Operating<br>Non-operating | 9843 ft (3,000 m)<br>40,000 ft (12,192 m) |
| Electrostatic immunity | 6 kV |

# Maintenance

The P6450 High-Density Logic Analyzer Probe does not require scheduled or periodic maintenance. Refer to the Functional Check section below to verify the basic functionality of the probes.

## Probe Calibration

To confirm that the probes meet or exceed the performance requirements for published specifications with a compatible logic analyzer module, you must return the probes to your local Tektronix service center.

## Functional Check

Connect the logic analyzer probes to a signal source and check for signal activity in the LA Setup window.

## Inspection and Cleaning

⚠ **CAUTION.** *To prevent damage during the probe connection process, do not touch the exposed edge of the interface clip. Do not drag the contacts against a hard edge or corner.*

To maintain a reliable electrical contact, keep the probes free of dirt, dust, and contaminants. Remove dirt and dust with a soft brush. Avoid brushing or rubbing the c-spring contacts. For more extensive cleaning, use only a damp cloth. Never use abrasive cleaners or organic solvents.

## Service Strategy

The P6450 probe uses replaceable c-spring cLGA clips. See page 30 for the replacement procedure. If a probe failure other than the cLGA clip occurs, return the entire probe to your Tektronix service center for repair.

### Replacing the cLGA Clip

For replacement part number information, refer to the Replaceable Parts list. (See Table 9 on page 32.) To replace the clip, do the following:

1. Gently pull one side of the clip away from the probe head and then remove the entire clip. (See Figure 19.)
2. Align the new clip with the probe head and gently snap it into place.
3. Test the probe to confirm that all channels are functional.

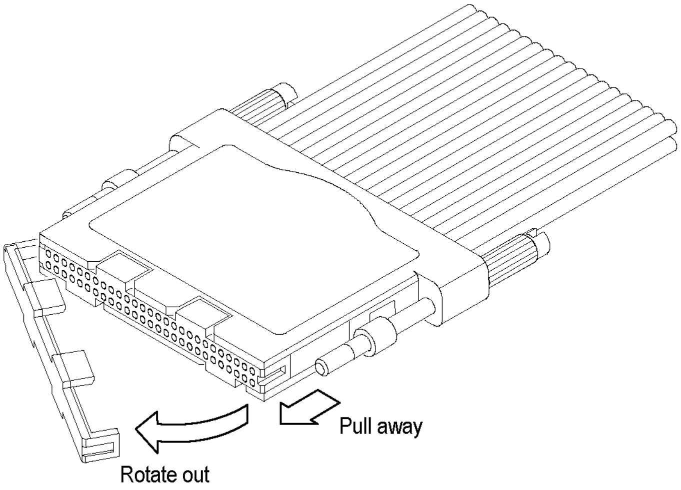


Figure 19: Replacing the cLGA clip

## Legacy Probe and Attachment Support

- Nexus Technology, a Tektronix Partner, sells accessories that allow you to use the P6450 probe with legacy attachment connectors.
- Please contact Nexus Technology directly for more information.
- Contact Information:

Nexus Technology

Phone: 877-595-8116

Fax: 877-595-8118

## Repackaging Instructions

Use the original packaging, if possible, to return or store the probes. If the original packaging is not available, use a corrugated cardboard shipping carton. Add cushioning material to prevent the probes from moving inside the shipping container.

Enclose the following information when shipping the probe to a Tektronix Service Center:

- Owner's address
- Name and phone number of a contact person
- Type of probe
- Reason for return
- Full description of the service required

# Replaceable Parts

This chapter contains a list of the replaceable components for the P6450 probe. Use this list to identify and order replacement parts.

## Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

## Using the Replaceable Parts List

### Replaceable Parts

TheP6450 probe contains only the cLGA clip as a replaceable part. If probe failure occurs, return the entire probe to your Tektronix service representative for repair.

Refer to the following list for replaceable items:

**Table 7: Parts list column descriptions**

| Column | Column name | Description |
|---|---|---|
| 1 | Figure & index number | Items in this section reference figure and index numbers to the exploded view illustrations that follow. |
| 2 | Tektronix part number | Use this part number when ordering replacement parts from Tektronix. |
| 3 and 4 | Serial number | Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers. |
| 5 | Qty | This indicates the quantity of parts used. |
| 6 | Name & description | An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification. |

### Table 7: Parts list column descriptions (cont.)

| Column | Column name | Description |
|---|---|---|
| 7 | Mfr. code | This indicates the code of the actual manufacturer of the part. |
| 8 | Mfr. part number | This indicates the actual manufacturer's or vendor's part number. |

## Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1-1972.

## Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

### Table 8: Manufacturers cross index

| Mfr. code | Manufacturer | Address | City, state, zip code |
|---|---|---|---|
| 80009 | TEKTRONIX INC | 14150 SW KARL BRAUN DR PO BOX 500 | BEAVERTON, OR 97077-0001 |

### Table 9: P6450 replaceable parts list

| Figure & index number | Tektronix part number | Serial no. effective | Serial no. discont'd | Qty | Name & description | Mfr. code | Mfr. part number |
|---|---|---|---|---|---|---|---|
| | | | | | P6450 STANDARD ACCESSORIES | | |
| | | | | | | | |
| 20-1 | 010-0775-10 | | | 1 | P6450 PROBE (INCLUDES SHEET OF LABELS) | 80009 | 010-0775-10 |
| -2 | 020-2622-00 | | | 2 | COMPONENT KIT, CLGA INTERFACE CLIP; 1 EA, SAFETY CONTROLLED | 80009 | 020-2622-00 |
| -3 | 200-4893-00 | | | 1 | COVER,PROTECTIVE; BLACK VINYL (PLASTISOL) WITH STATIC-DISSIPATIVE ADDITIVE | 80009 | 200-4893-00 |
| -4 | 020-2908-00 | | | 1 | PPIMARY P69XX RETENTION KIT, QTY 2 CONNECTORS | 80009 | 020-2908-00 |
| | 020-2539-00 | | | 1 | KIT, RETENTION; P6450 | 80009 | 020-2539-00 |
| | 346-0300-00 | | | 1 | STRAP,VELCRO;ONE WRAP,BLACK,0.500W X 8.00L,QTY 2 BAGGED & LABELED | 80009 | 346-0300-00 |
| | 003-1890-00 | | | 1 | TOOL,HAND; USED TO TIGHTEN PROBE HEAD TO DUT | 80009 | 003-1890-00 |
| | 071-2478-XX | | | 1 | MANUAL, TECH; INSTRUCTION, P6450 HIGH DENSITY LOGIC ANALYZER PROBE | 80009 | 071-2478-XX |
| | 335-1990-00 | | | 1 | P6450 PROBE, SHEET OF LABELS | 80009 | 335-1990-00 |

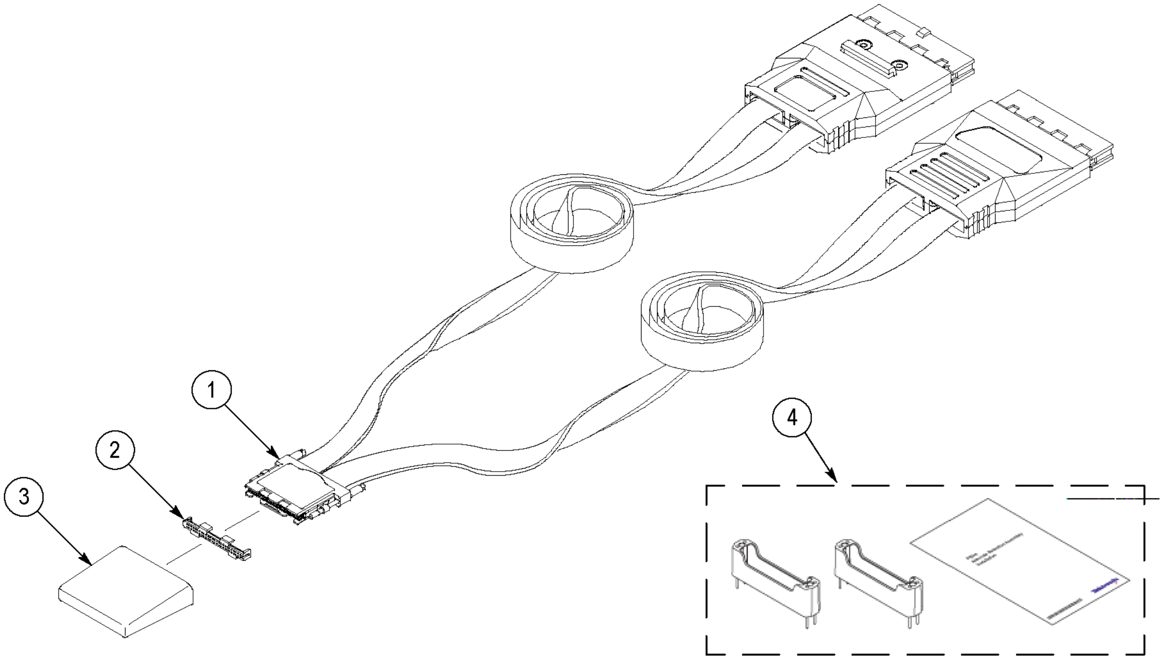


Figure 20: P6450 High-Density probe accessories

### Table 10: P6450 Probe optional accessories

| Figure & index number | Tektronix part number | Serial no. effective | Serial no. discont'd | Qty | Name & description | Mfr. code | Mfr. part number |
|---|---|---|---|---|---|---|---|
| 21-1 | 196-3494-00 | | | 1 | FLYING LEADSET | 80009 | 196-3494-00 |
| -2 | SMG50 | | | 2 | ADAPTER KIT; BAG OF 20 KLIPCHIP ADAPTER (40 TOTAL) | 80009 | SMG50 |
| -3 | 020-2908-00 | | | 1 | P69xx ALTERNATE RETENTION ASSEMBLY KIT, QTY 2 | 80009 | 020-2908-00 |
| -4 | 020-2910-00 | | | 1 | P69xx ALTERNATE RETENTION ASSEMBLY KIT, QTY 50 | 80009 | 020-2910-00 |
| -5 | 020-2539-00 | | | 1 | KIT, RETENTION; P6960/P6980 | 80009 | 020-2539-00 |

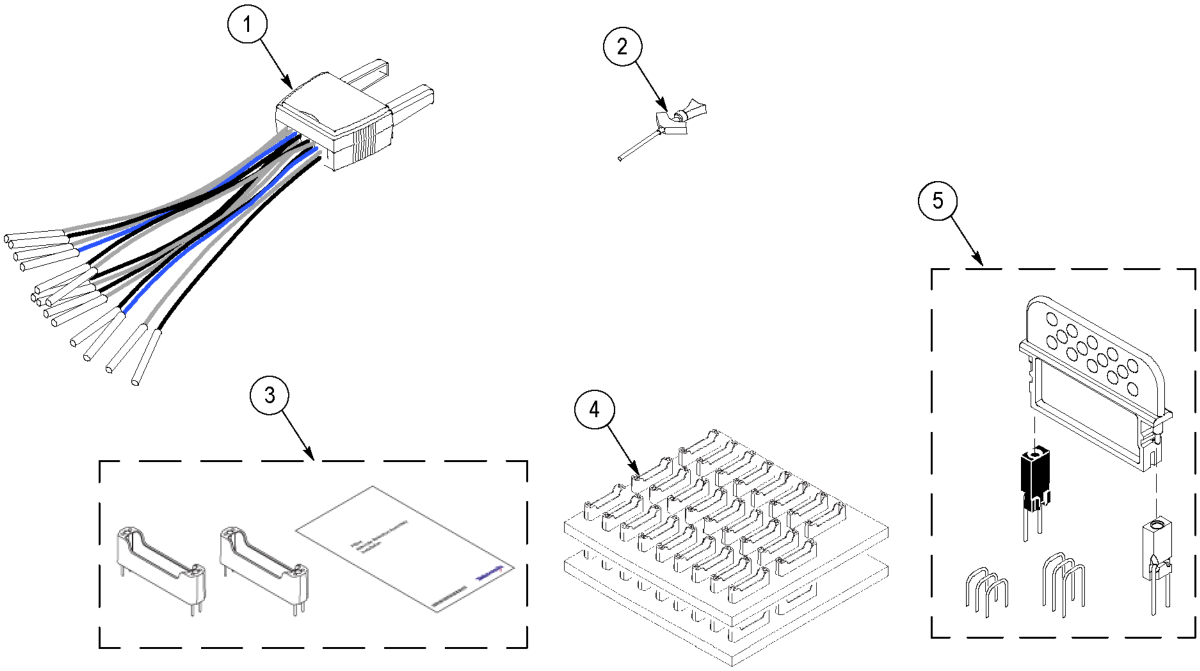


Figure 21: Optional accessories

# Index