Product Specification

Bi-Color OLED Display

Part Number: **FDS128x64(26.7x31.26)TFP**

PREPARED BY	CHECKED BY	APPROVED BY

Focus Display Solutions, Inc.

Notes:

1. Please contact Focus Display Solutions, Inc. before assigning your product based on this module specification

2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Focus Display Solutions, Inc. For any intellectual property claims or other problems that may result from application based on the module described herein

1 Overview

FDS128x64(26.7x32.76)TFP is an area color OLED display module with 128×64 dot matrix. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

2 Features

Display Color: Yellow & Blue

Dot Matrix: 128×64

Driver IC: SSD1306Z

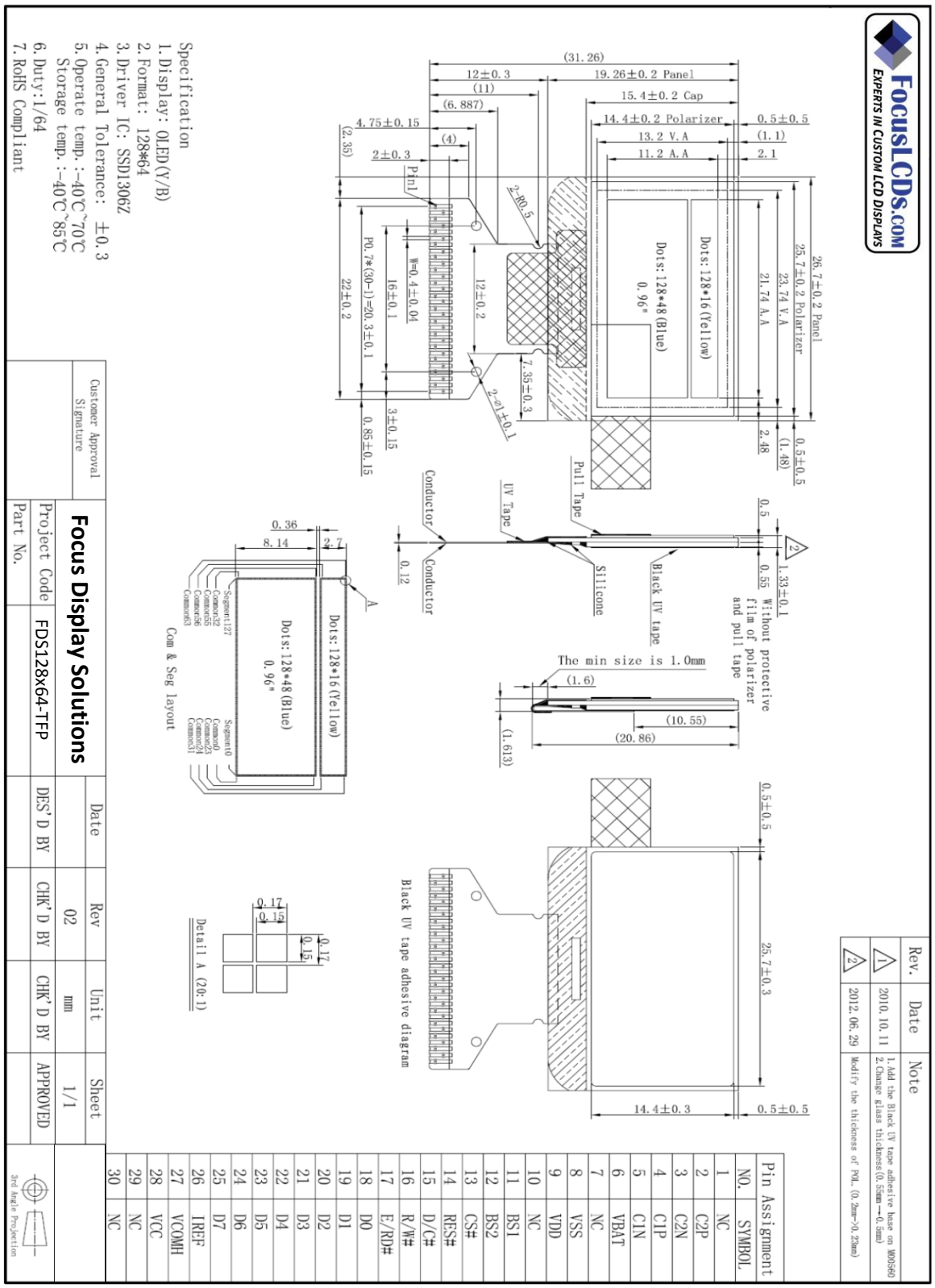
Interface: 8-bit 6800, 8-bit 8080, I 2C, 4-Wire SPI

Wide range of operating temperature: -40℃ to 70℃

3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W)×64(H)	-
2	Dot Size	0.15(W)×0.15 (H)	mm2
3	Dot Pitch	0.17(W)×0.17 (H)	mm2
4	Aperture Rate	78	%
5	Active Area	21.74(W)×11.2 (H)	mm2
6	Panel Size	26.7(W)×19.26(H)×1.05(T)	mm3
7	Module Size	26.7(W)×31.26(H)×1.33(T)	mm3
8	Diagonal A/A Size	0.96	inch
9	Module Weight	1.32±10%	gram

4 Mechanical Drawing



5 Module Interface

<table>
<tr><th>PIN No</th><th>PIN Name</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>NC</td><td>No Connection</td></tr>
<tr><td>2</td><td>C2P</td><td rowspan="2">The PIN for charge pump capacitor; Connect to each other with a capacitor.</td></tr>
<tr><td>3</td><td>C2N</td></tr>
<tr><td>4</td><td>C1P</td><td rowspan="2">The PIN for charge pump capacitor; Connect to each other with a capacitor.</td></tr>
<tr><td>5</td><td>C1N</td></tr>
<tr><td>6</td><td>VBAT</td><td>Power supply for charge pump regulator circuit.
<table>
<tr><th>Status</th><th>VBAT</th><th>VDD</th><th>VCC</th></tr>
<tr><td>Enable Charge Pump</td><td>Connect to external VBAT source</td><td>Connect to external VCC source</td><td>A capacitor should be connected between this Pin and VSS</td></tr>
<tr><td>Disable Charge Pump</td><td>Keep float</td><td>Connect to external VCC source</td><td>Connect to external VCC source</td></tr>
</table></td></tr>
<tr><td>7</td><td>NC</td><td>No Connection</td></tr>
<tr><td>8</td><td>VSS</td><td>Ground</td></tr>
<tr><td>9</td><td>VDD</td><td>Power supply Pin for core logic operation</td></tr>
<tr><td>10</td><td>NC</td><td>No Connection</td></tr>
<tr><td>11</td><td>BS1</td><td rowspan="2">Table 5-1</td></tr>
<tr><td>12</td><td>BS2</td></tr>
<tr><td>13</td><td>CS#</td><td>Chip Select, active LOW</td></tr>
<tr><td>14</td><td>RES#</td><td>This Pin is reset signal input. When the Pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to VDD) during normal operation.</td></tr>
<tr><td>15</td><td>D/C#</td><td>This is Data/Command control pin. When it is pulled HIGH (i.e. connect to VDD), the data at D[7:0] is treated as data. When it pulled LOW, the data at D[7:0] will be transferred to the command register.
In IC mode, this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>16</td><td>R/W#</td><td>This is read/write control input pin connecting to the MCU interface.
When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to VDD) and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or IC interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>17</td><td>E/RD#</td><td>When interfacing to a6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH (i.e. connect to VDD) and the chip is selected.
When connecting to an 8080-series microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or IC interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>18~25</td><td>D0-D7</td><td>These are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus.
When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC.
When IC mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.</td></tr>
</table>

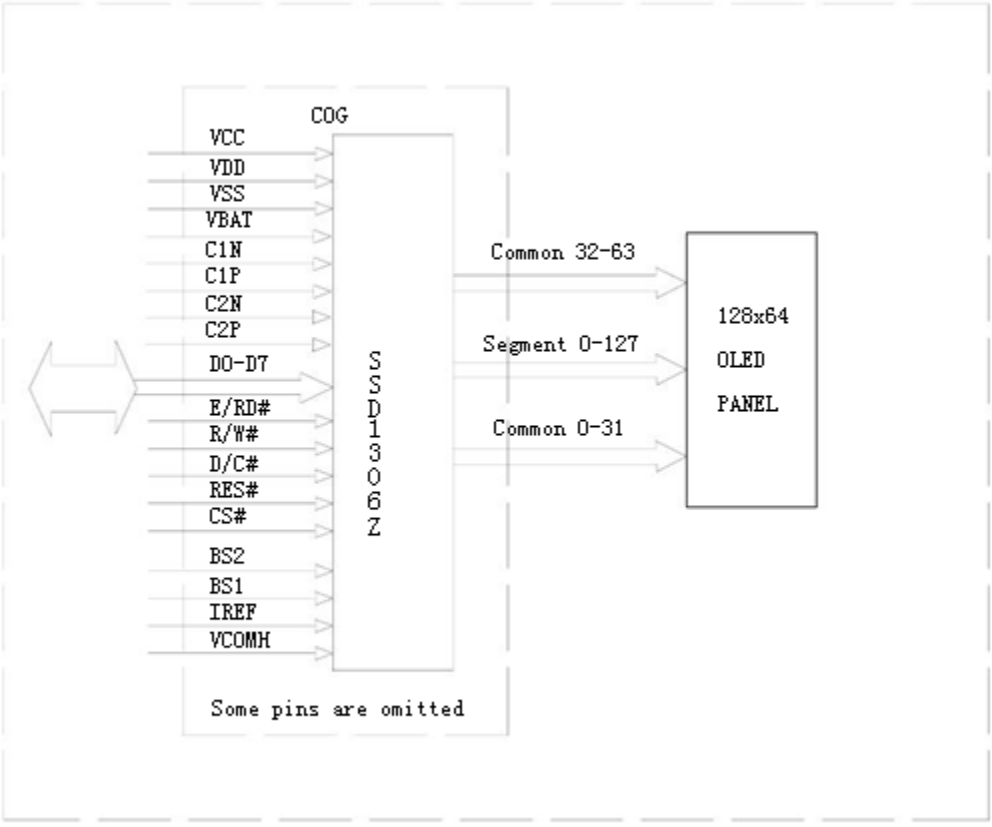
PIN No	PIN Name	DESCRIPTION *(CONTINUED…)*
26	IREF	Segment output current reference pin
27	VCOMH	Common signal deselected voltage level. Connected a capacitor to VSS.
28	VCC	Power supply for panel driving voltage
29~30	NC	No Connection

Table 5-1: MCU Bus Interface Pin Selection

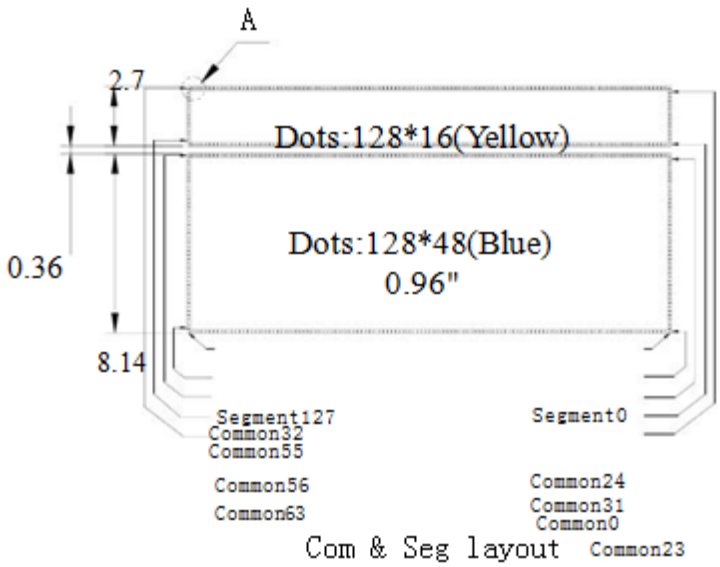
Pin Name	IC	6800	8080	4-SPI
BS1	1	0	1	0
BS2	0	1	1	0

6 Function Block Diagram

6.1 Function Block Diagram



6.2 Panel Layout Diagram



7 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	VDD	-0.3	4	V	IC maximum rating
Charge Pump Regulator Supply Voltage	VBAT	-0.3	5.0	V	IC maximum rating
OLED Operating voltage	VCC	0	16	V	IC maximum rating
Operating Temp	Top	-40	70	℃	-
Storage Temp	Tstg	-40	85	℃	-

Note (1): All of the voltages are on the basis of "VSS = 0V".

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 "Electrical Characteristics". Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions

8 Electrical Characteristics

8.1 DC Electrical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYPE	MAX	UNIT
Logic Supply Voltage	VDD	22±3°C, 55±15%R.H	1.65	3.0	3.3	V
OLED Driver Supply Voltage (Supply Externally)	VCC	22±3°C, 55±15%R.H	7	7.2	7.5	V
OLED Driver Supply Voltage (Generated by Internal DC/DC)	VCC	22±3°C, 55±15%R.H	7	7.2	7.5	V
Charge Pump Regulator Supply Voltage	VBAT	22±3°C, 55±15%R.H	3.3	3.7	4.2	V
High-level Input Voltage	VIH	-	0.8×VDD	-	-	V
Low-level Input Voltage	VIL	-	-	-	0.2×VDD	V
High-level Output Voltage	VOH	-	0.9×VDD	-	-	V
Low-level Output Voltage	VOL	-	-	-	0.1×VDD	V

Note : The VCC input must be kept in a stable value; ripple and noise are not allowed.

8.2 Electro-optical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYPE	MAX	UNIT
Normal Mode Brightness	Lbr	All pixels ON(1) (VCC generated by internal DC/DC)	50	70	--	cd/m
ICC Sleep mode Current	ICC,SLEEP	VDD=1.65V~3.3V, VCC=7V~15V, Display OFF, No panel attached	--	--	20	uA
IDD, Sleep mode Current	IDD,SLEEP	VDD=1.65V~3.3V, VCC=7V~15V, Display OFF, No panel attached	--	--	20	uA
Normal Mode Power Consumption	Pt	All pixels ON(1)	--	88.8	107.3	mW
C.I.E.(Blue)	(x)	x,y(CIE1931)	0.12	0.16	0.20	--
	(y)		0.23	0.27	0.31	--
C.I.E.(Yellow)	(x)		0.47	0.51	0.55	--
	(y)		0.44	0.48	0.52	--
Dark Room Contrast	CR	--	≥2000:1	--	--	--
Response Time	--	--	--	10	--	Us
View Angle	--	--	≥160	--	--	Degree

8.2 Note(1): Normal Mode test conditions are as follows:
- Driving voltage : 7.2V(VCC Supplied Externally) or VBAT:3.7V(VCC Generated by Internal DC/DC).
- Contrast setting : 0XCF; Frame rate : 105Hz; Duty setting : 1/64

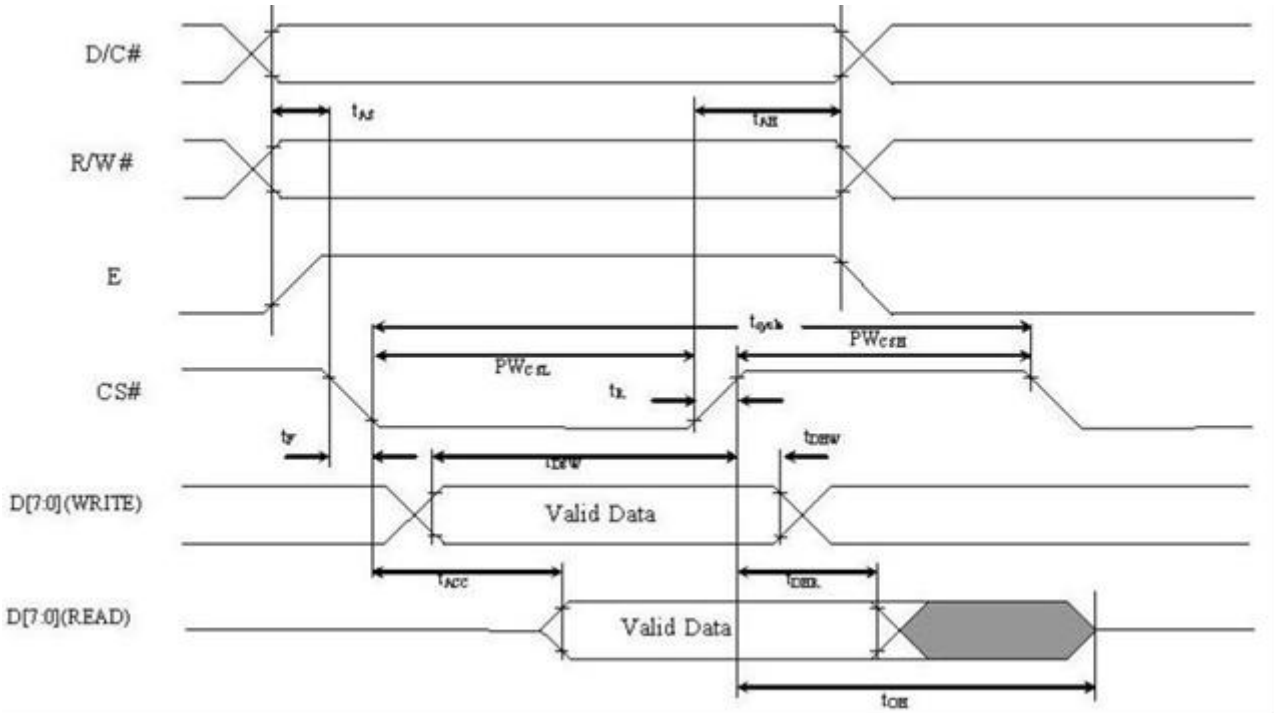
8.3 AC Electrical Characteristics

(1)6800-Series MPU Parallel Interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

6800-series MCU parallel interface characteristics



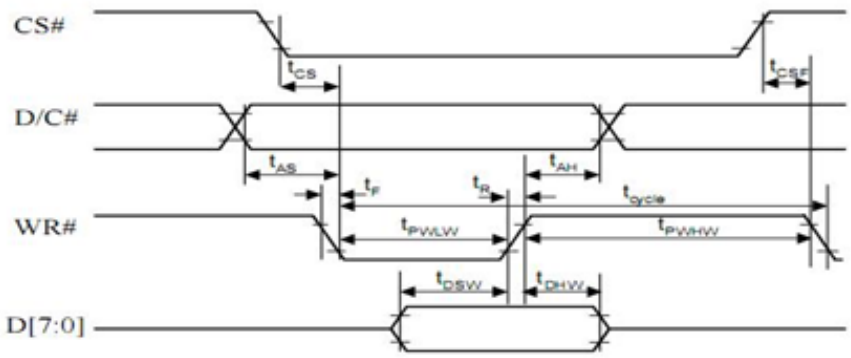
(2)8080-Series MPU Parallel Interface Timing Characteristics

(VDD - VSS = 1.65V to 3.3V, TA = 25°C)

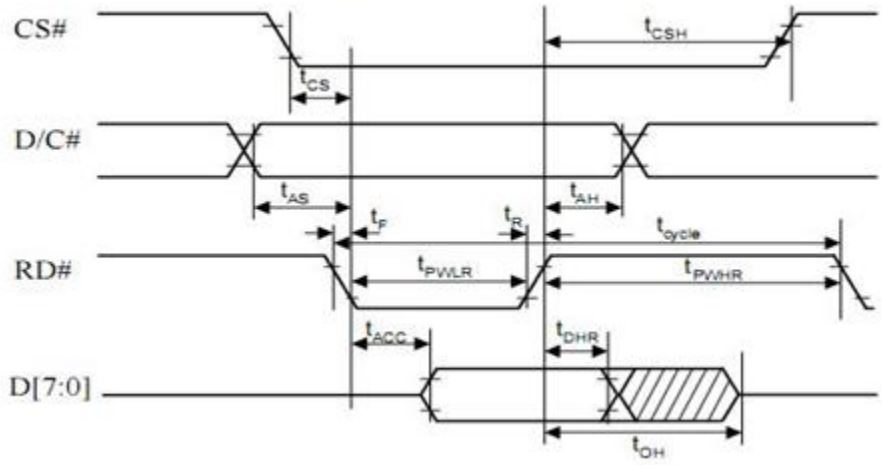
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics

Write Cycle



Read cycle



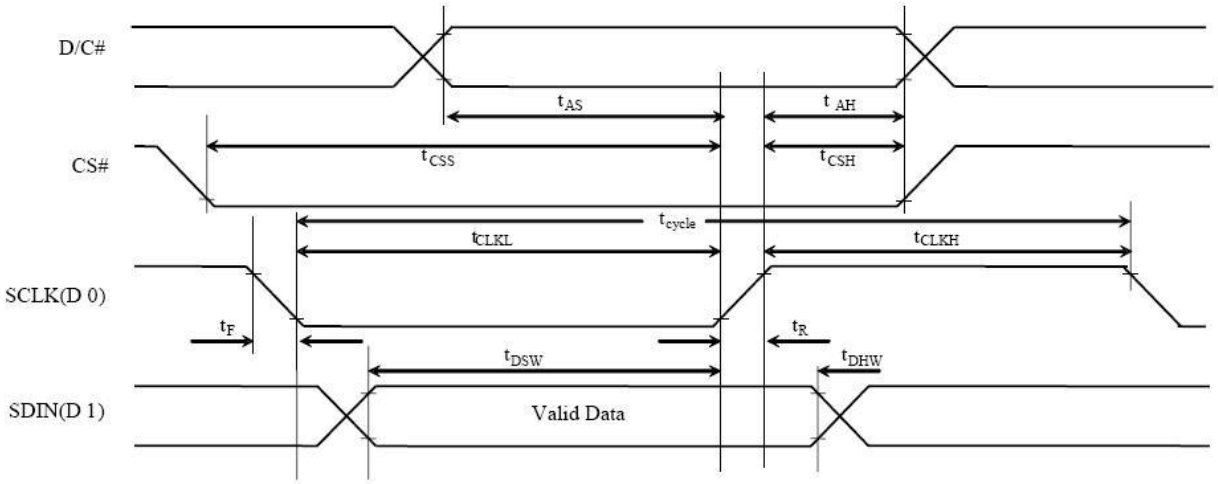
(3)4-Wire Series Interface Timing Characteristics

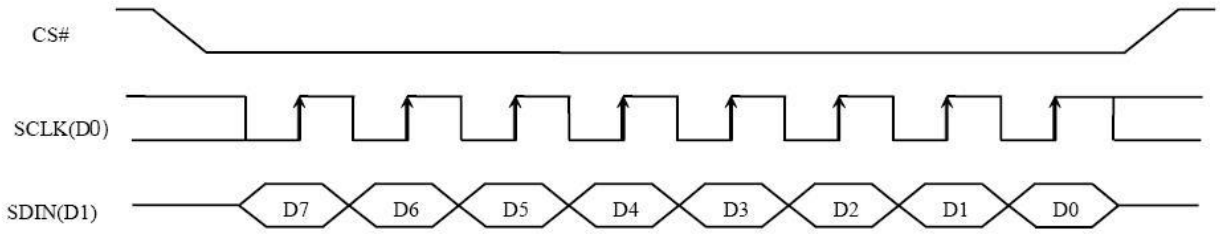
(VDD - VSS = 1.65V to 3.3V, TA = 25°C)

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

4-wire Serial interface characteristics





(4) I 2C Interface Timing Characteristics
(VDD - VSS = 1.65V to 3.3V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I 2C Interface Timing Characteristics