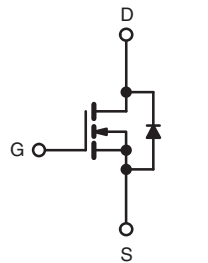
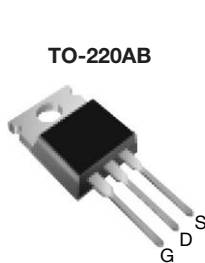


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	1.2
$Q_g$ (Max.) (nC)	42	
$Q_{gs}$ (nC)	10	
$Q_{gd}$ (nC)	20	
Configuration	Single	



N-Channel MOSFET

### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{oss}$  Specified
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

### TYPICAL SMPS TOPOLOGIES

- Single Transistor Forward

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFBC40APbF SiHFBC40A-E3
SnPb	IRFBC40A SiHFBC40A


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	600	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	A	
		$T_C = 100$ °C		
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	25		
Linear Derating Factor		1.0	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	570	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	6.2	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	13	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	125	W
Peak Diode Recovery $dV/dt^c$	$dV/dt$	6.0	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw	10		lbf · in
		1.1	N · m	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25$  °C,  $L = 29.6$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 6.2$  A (see fig. 12).
- $I_{SD} \leq 6.2$  A,  $dI/dt \leq 80$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.66	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3.7\text{ A}^b$	-	-	1.2	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 3.7\text{ A}$	3.4	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	1036	-	pF
Output Capacitance	$C_{oss}$		-	136	-	
Reverse Transfer Capacitance	$C_{rss}$		-	7.0	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	1487	-
			$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	36	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$			-	48	-
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 6.2\text{ A}, V_{DS} = 480\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	42	nC
Gate-Source Charge	$Q_{gs}$		-	-	10	
Gate-Drain Charge	$Q_{gd}$		-	-	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 6.2\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 47\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	13	-	ns
Rise Time	$t_r$		-	23	-	
Turn-Off Delay Time	$t_{d(off)}$		-	31	-	
Fall Time	$t_f$		-	18	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	6.2	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	25	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 6.2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 6.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	431	647	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	1.8	2.8	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

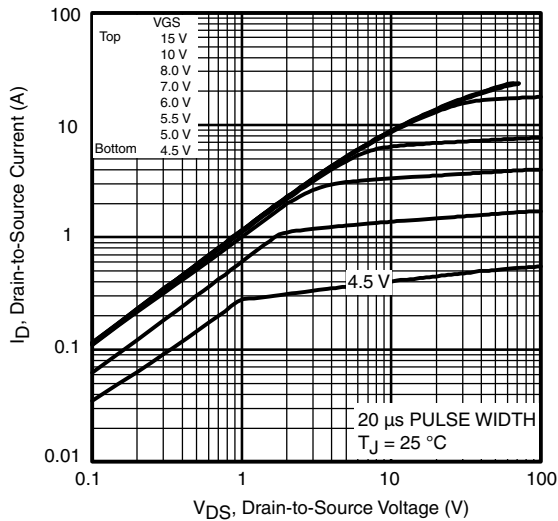


Fig. 1 - Typical Output Characteristics

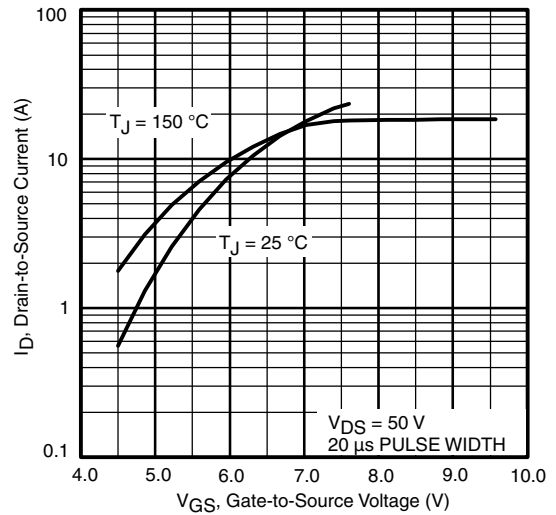


Fig. 3 - Typical Transfer Characteristics

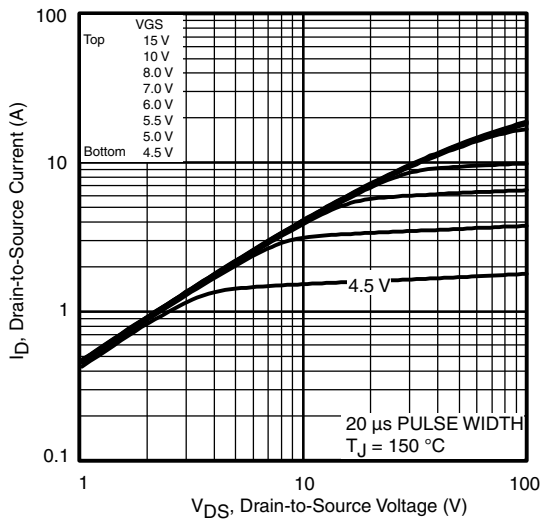


Fig. 2 - Typical Output Characteristics

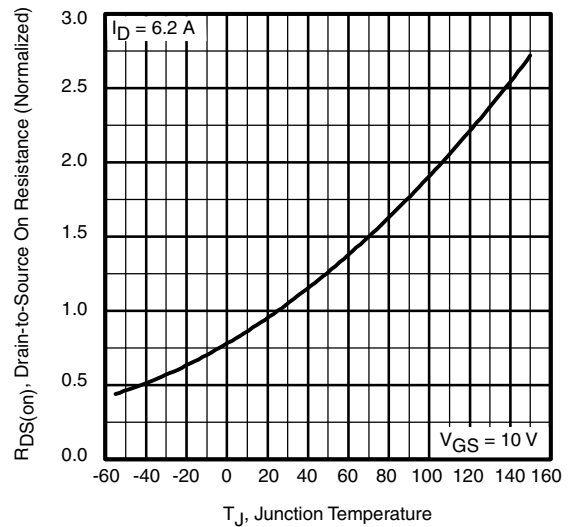
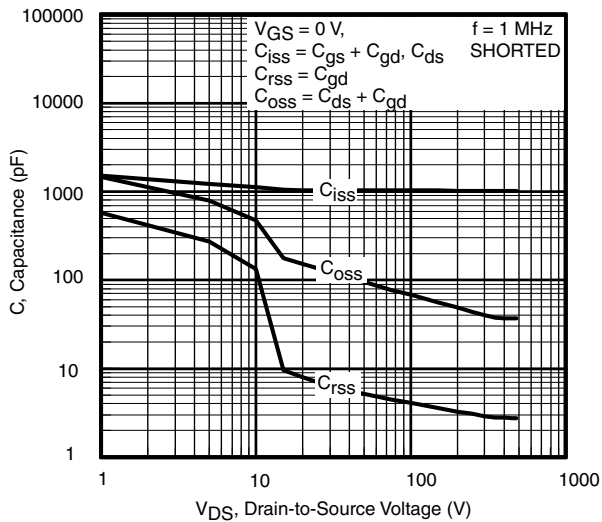
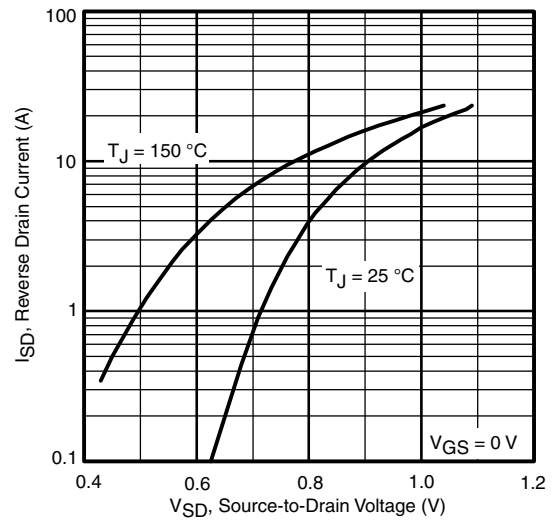


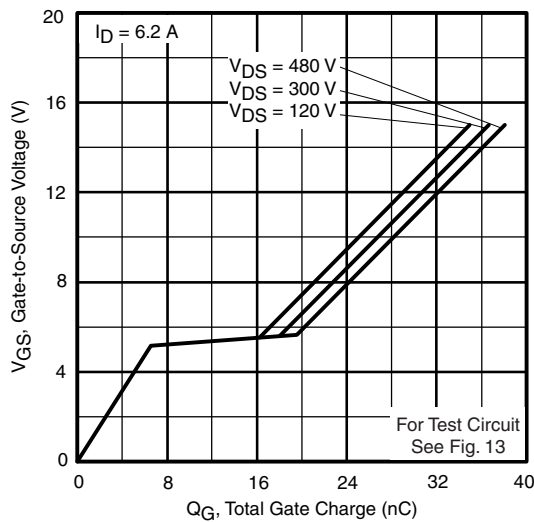
Fig. 4 - Normalized On-Resistance vs. Temperature



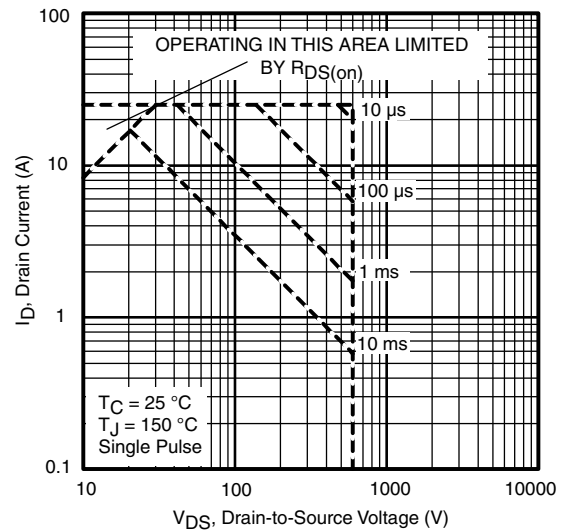
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



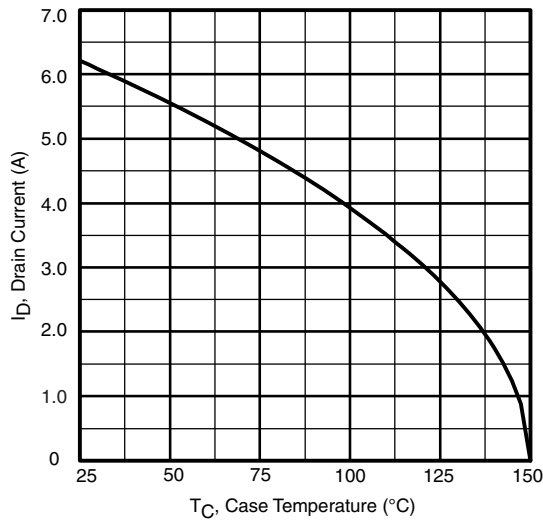
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



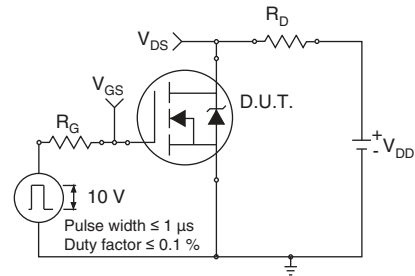
**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



**Fig. 8 - Maximum Safe Operating Area**



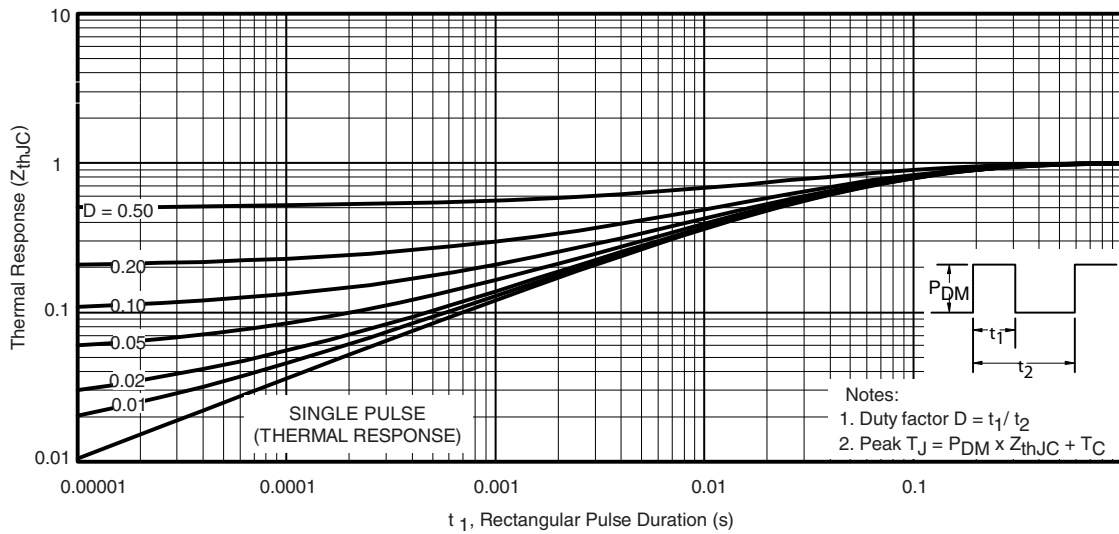
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



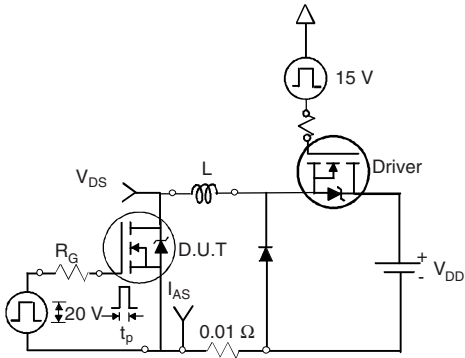
**Fig. 10a - Switching Time Test Circuit**



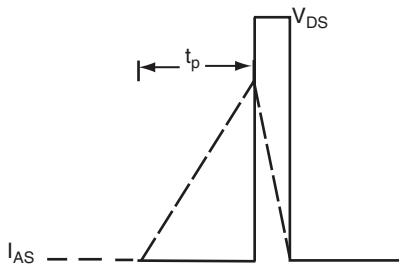
**Fig. 10b - Switching Time Waveforms**



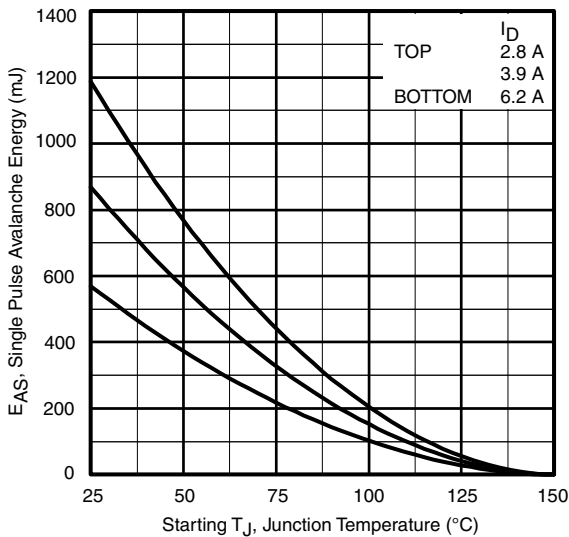
**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



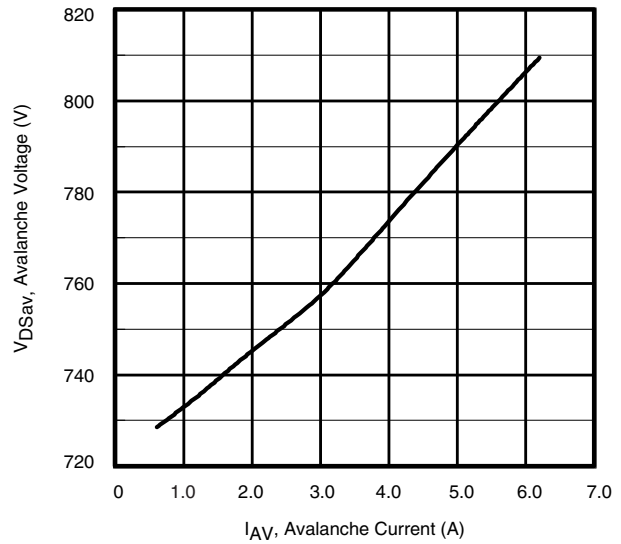
**Fig. 12a - Unclamped Inductive Test Circuit**



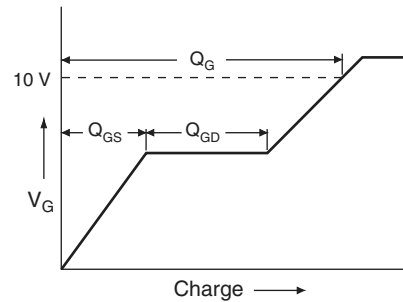
**Fig. 12b - Unclamped Inductive Waveforms**



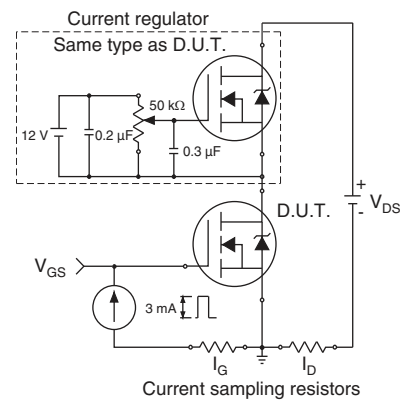
**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**



**Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current**



**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**

### Peak Diode Recovery dV/dt Test Circuit



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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## TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15  
DWG: 6031

**Note**

- M\* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM







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