Product Specification

Part Number: FDS20x2(116x37)TBP

Revision: Ver 1.0

Issue Date: 3/29/2014

Approved By	Review By	Prepared By
	Control Document ☐ Yes ☐ No	
	Confidential Document ☐ Yes ☐ No	

1.Module Basic Specification

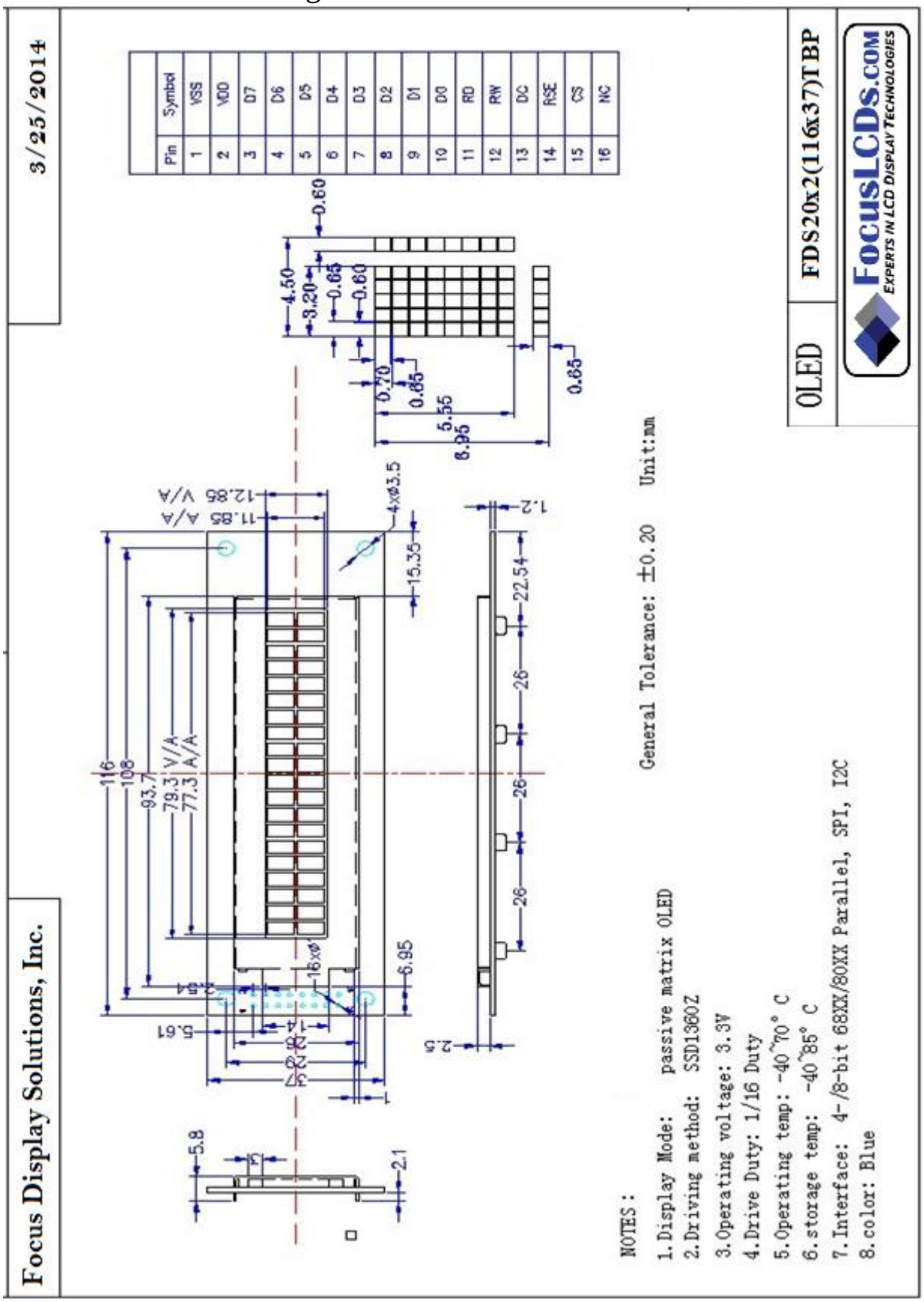
1.1 Display Specifications

1) Display Mode: Passive Matrix OLED
2) Display Color: White
3) Drive Duty: 1/16 Duty
4) Controller Driver: SSD1360Z

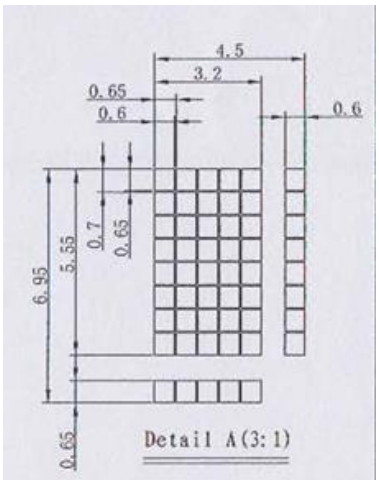
1.2 Module Features

Items	Specification	Unit
Diagonal A/A Size	3.05	Inch
Number of dots	20 Characters (5x8 dots)x2 Lines	dot
Module size	116 x 37 x 5.8	mm
Active Area	77.3 x 11.85	mm
viewing Area	79.3 x 12.85	mm
Character Pitch	3.9 x 6.3	mm
Character Size	3.2 x 5.55	mm
Dot Pitch	0.65 x 0.70	mm
Dot Size	0.60x 0.65	mm
General Tolerance	±0.20	mm

1.3 Mechanical Drawing



1.4 - Active Area / Address Mapping & Character Construction



	1	2	3	4	5	6	7	8	9	10	11	12	13
LINE1	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h
LINE2	44h	45h	46h	47h	48h	49h	4Ah	4Bh	4Ch	4Dh	4Eh	4Fh	50h

	14	15	16	17	18	19	20
LINE1	11h	12h	13h	14h	15h	16h	17h
LINE2	51h	52h	53h	54h	55h	56h	57h

1.5 Pin Definition

Pin number	Symbol	Type	Function
1	VSS	P	Power supply ground
2	VDD	P	3.3V power supply
3~10	D7~D0	I/O	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.When I2C mode is selected, D2 & D1 should be tired together and serve as SDA-out & SDA-in in application and D0 is the serial clock input SCL.
11	RD	I	When interface to a 6800-series microprocessor, this pin will be used as the Enable (E) signal, When interface to an 8080-microprocessor, this pin receives the Read(RD#)signal.
12	RW	I	This is read/write control input pin connecting to the MCU interface. When interface to a 6800-series microprocessor, Read mode will be carried out when this pin is pulled HIGH and write mode when low .When interface to an 8080-microprocessor, this pin will be the data Write input. When serial interface is selected, this pin must be connected to Vss
13	DC	I	This is DATA/COMMAND control pin. When it is pulled HIGH, the data at D[0~7] is treated as data. When it is pulled LOW, the data at D[0~7] will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
14	RSE	I	This pin is reset signal input (active LOW)
15	CS	I	This pin is chip select input (active LOW)

1.6 Jump

BS0 /BS1 /BS2:MUC bus interface selection pin.

BS2	BS1	BS0	Interface
0	0	0	Serial Interface
0	1	0	I^2C
1	0	0	8-bit 6800 parallel
1	1	0	8-bit 6800 parallel

Notes: "0"connection GND and "1"connection VDD.

SPI and I2C interface version PCB are available

2.Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for logic	V_{DD}	-0.3	3.6	V	1,2
Supply Voltage for display	V_{CC}	0	13	V	1,2
Operating Temperature	TOP	-40	70	°C	-
Storage Temperature	TSTG	-40	85	°C	-
Life time (100cd/m²)(white)		20000	-	hour	3

Notes1:

All the above voltages are on the basis of "Vss =0V "

Notes2:

When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur, also for normal operations, it is desirable to use this module under the conditions according to Section 3."Optics and Electrical Characteristics "If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Notes3:

V_{CC} = 7.25V, Ta = 25° C, 50% Checkerboard.
Software configuration follows Section 6.4 Initialization. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3.Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note4	120	150	-	cd/m^2
C.I.E(White)	(x) (y)	C.I.E 1931	0.26 0.28	0.30 0.32	0.34 0.36	
Dark Room Contrast	CR		-	10,000:1	-	
View Angle			-	Free	-	degree

Optical measurement taken at V_{DD} =2.8V, V_{CC} =7.25V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}	InternalRegulatorEnable(Output)	-	3.3	-	V
		InternalRegulatorDisable(Input)	2.4	-	3.6	V
Supply Voltage for I/O	V_{DDIO}	5V Voltage Mode	4.4	-	5.5	V
		Low Voltage Mode	2.4	-	3.6	V
Supply Voltage for Display	V_{CC}	Note4	7	12	12.5	V
High Level Input	V_{IH}	-	$0.8\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}	-	0	-	$0.2\times V_{DDIO}$	V
High Level Output	V_{OH}	I_{OUT}=100μA,3.3MHz	$0.9\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{OUT}=100μA,3.3MHz	0	-	$0.1\times V_{DDIO}$	V
Operating Current for V_{DD}	I_{DD}	-	-	180	300	μA
Operating Currentfor V_{CC} (V_{CC} Supply Externally)	I_{CC}	Note5	-	16	21	mA
		Note6	-	27	32	mA
Sleep Mode Current for V_{DD}	$I_{DD,SLEEP}$	-	-	1	10	μA
Sleep Mode Current for V_{CC}	$I_{CC,SLEEP}$	-	-	2	10	μA

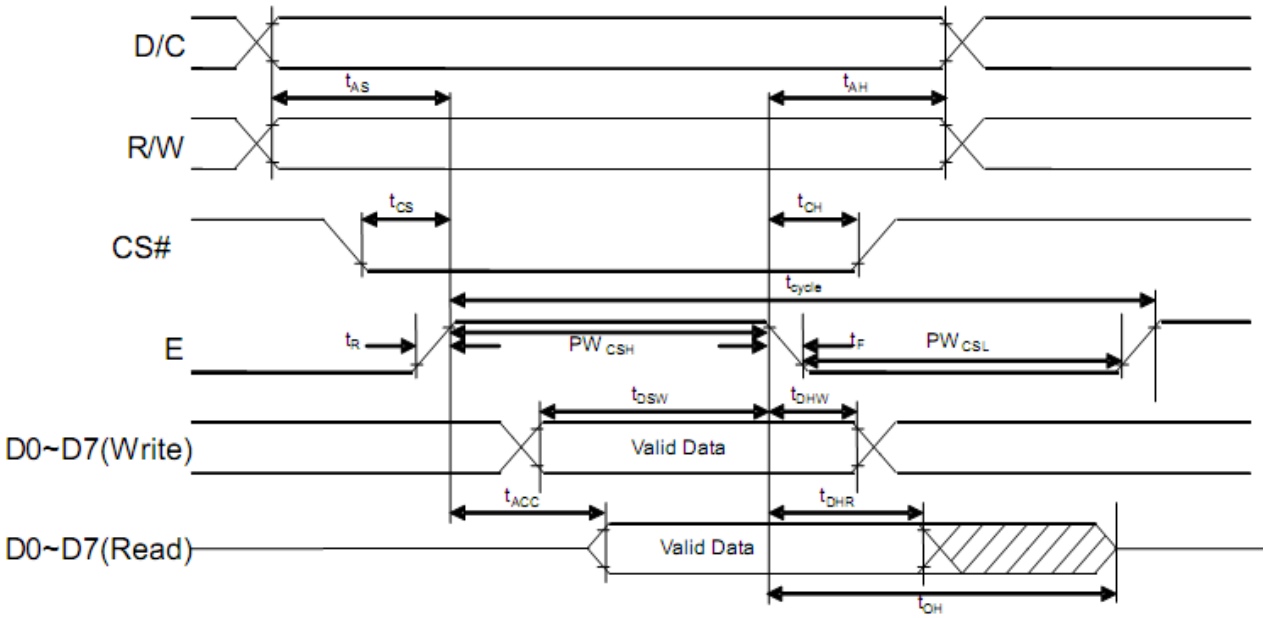
Note 4: VDD =2.8V,VCC =12V, 30% Display Area Turn on.
Note 5: VDD =2.8V,VCC =12V, 100% Display Area Turn on.
Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

(TA=25°C, V_{DD} -V_{SS}=1.65V to 3.3V)

Symbol	Parameter	Min	Type	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup time	13	-	-	ns
t_{AH}	Address Hold time	17	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	90	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM)	250	-	-	ns
	Chip Select Low Pulse Width (read command)	250	-	-	ns
	Chip Select Low Pulse Width (write)	50	-	-	ns
PW_{CSH}	Chip select High Pulse Width (read)	155	-	-	ns
	Chip Select High Pulse Width (write)	55	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

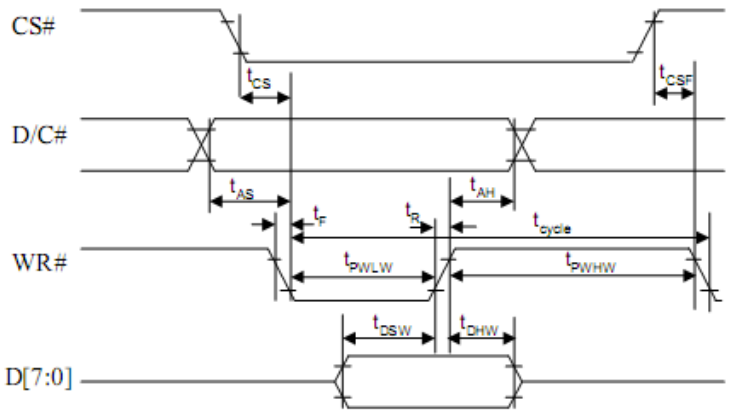


3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

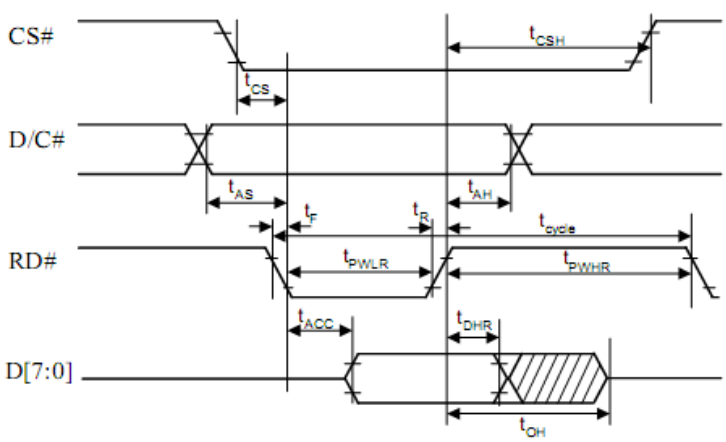
(TA=25°C, V_{DD} -V_{SS}=1.65V to 3.3V)

Symbol	Parameter	Min	Type	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup time	13	-	-	ns
t_{AH}	Address Hold time	17	-	-	ns
t_{CS}	Chip Select time	0	-	-	ns
t_{CSH}	Chip select Hold Time To read signal	0	-	-	ns
t_{CSF}	Chip select hold time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	200	ns
t_{PWLR}	Read Low time	250	-	-	ns
t_{PWLW}	Write Low time	50	-	-	ns
t_{PWHR}	Read High time	155	-	-	ns
t_{PWHW}	Write High time	55	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Write cycle



Read Cycle



4. Functional Specification

4.1 Commands

Command	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H", return cursor to its original position, if shifted. The contents of DDRAM are not changed.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor / blink moving direction with DDRAM address: I/D = "1": cursor/ blink moves to right & DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left & DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR).
Cursor or Display Shif	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left
Function set	0	0	0	0	1	DL	N	RE	BR1	BR0	Parallel bus width, DL when DL= "1" (POR): 8-bit, when DL = "0": 4-bit Numbers of display line, N when N = "1" (POR): 2-line, when N = "0": 1-line Extension register, RE ("0") Brightness ratio, BR[1:0] (% setting of different contrast level) 00: 100%, 01: 75%, 10: 50%, 11: 25%
Set CGRAM address	0	0	0	1	Character Generator (CG) RAM Address						Set CGRAM address in address counter. (POR=00 0000)
Set DDRAM Address	0	0	1	Display Data (DD) RAM Address / Cursor Address							Set DDRAM address in address counter. (POR=000 0000)
Write data	1	0	Write Data								Write data into internal RAM (DDRAM / CGRAM).
Read Data	1	1	Read Data								Read data from internal RAM (DDRAM / CGRAM).

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms (When V_{CC} is stable)
7. Send Display on command

4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms (When V_{CC} has reach 0 and panel is completely discharged)
4. Power down V_{DD}

Note **:**

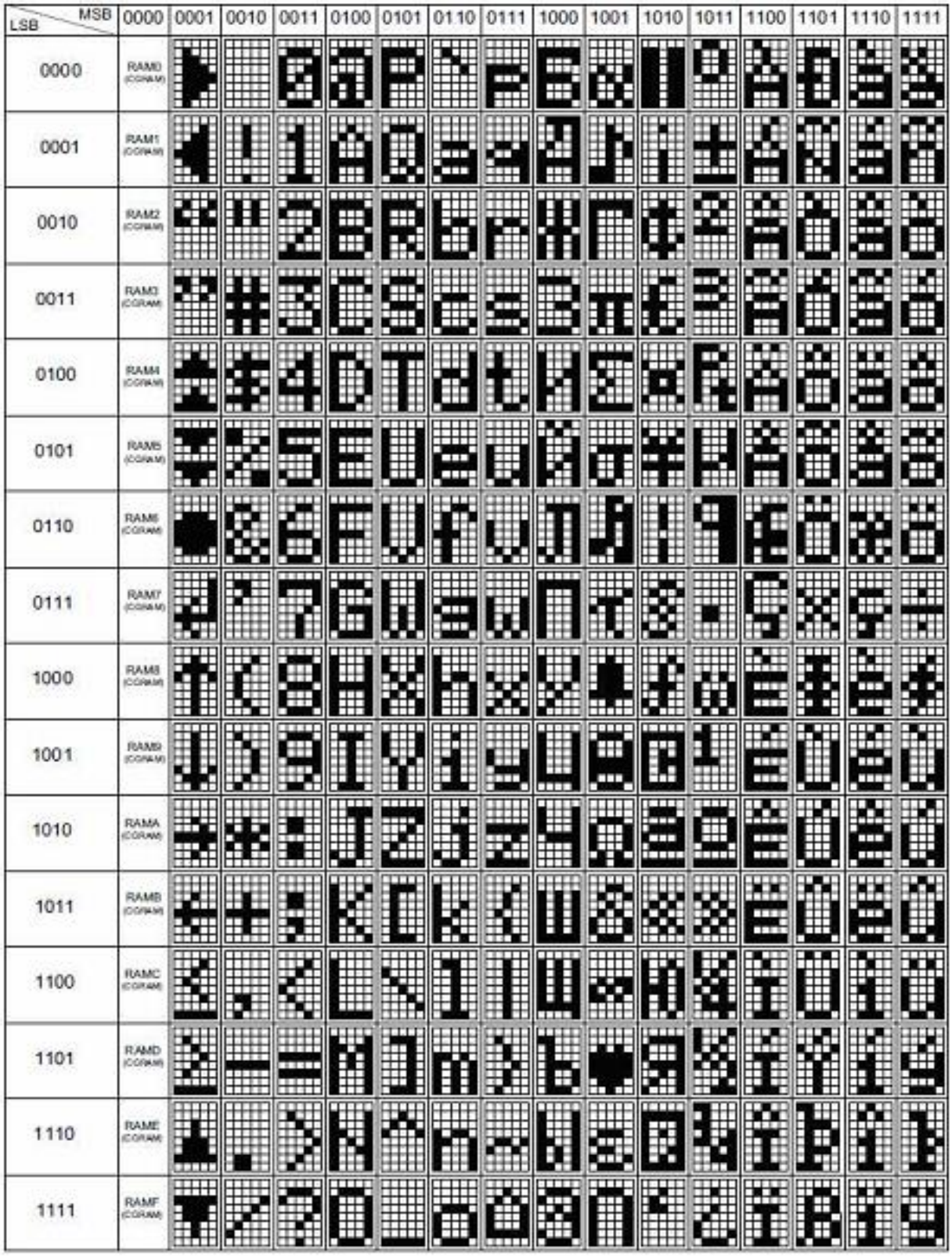
1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} power down.

4.3 **OLED Init_IC**

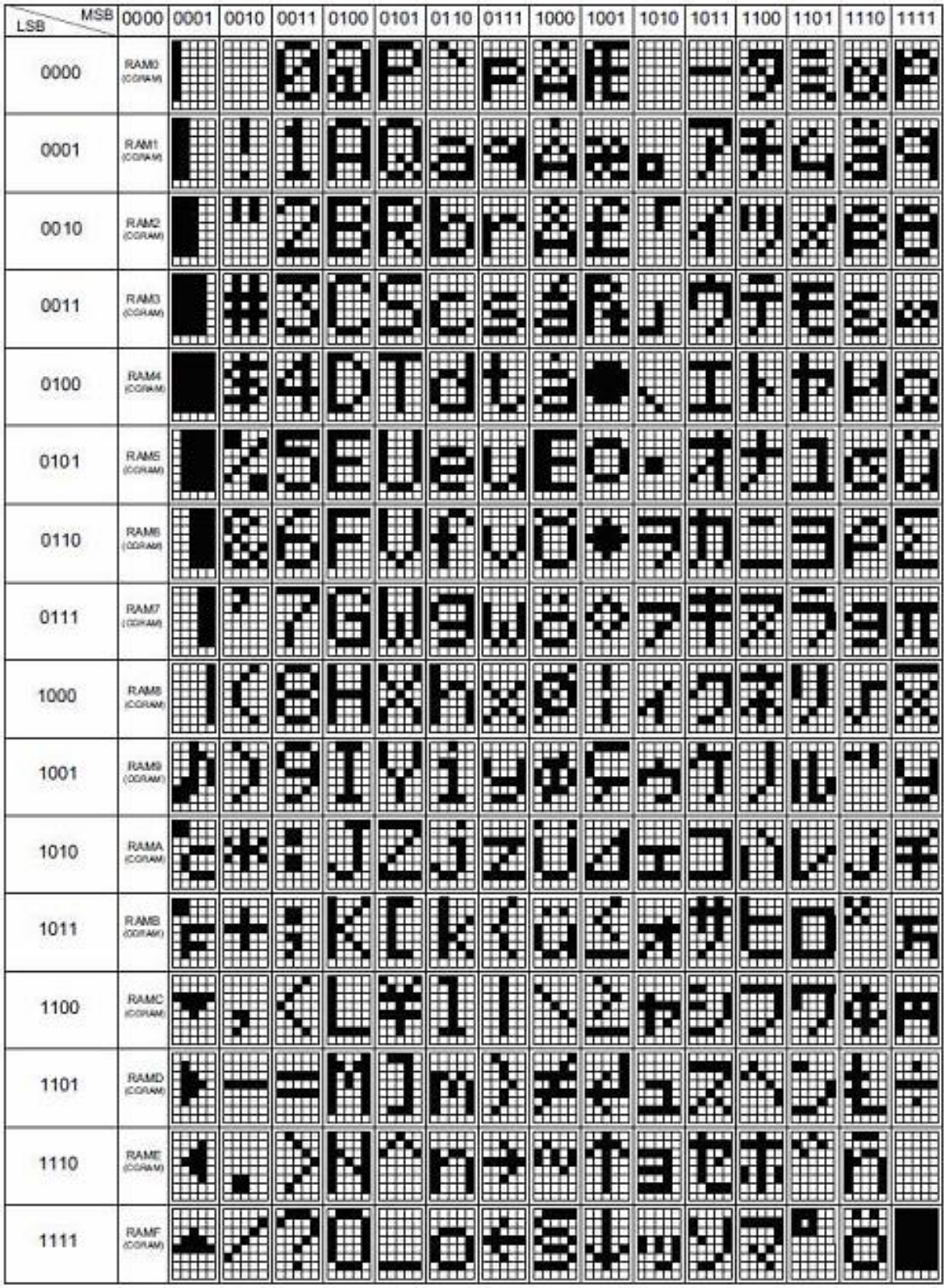
```
Void Init_IC( )
{
    Write_Command(0x01);    Write_Data(0x20);    //Clear Display
    Write_Command(0x02);      // Return Home
    Write_Command(0x06);      // Entry Mode Set
    Write_Command(0x0c);      // Display ON /OFF Control

    Write_Command(0xD3);      // Set Display Offset
    Write_Command(0x00);
    Write_Command(0x40);      // Set Display Start Line

    Write_Command(0X38);      // Function Set
    Write_Command(0x3c);      // Function Set re


    Write_Command(0x71);      // Function Selection A
    Write_Data(0x00);

    Write_Command(0x72);      // Function Selection B
    Write_Data(0x04);

    Write_Command(0x79);      // OLED characterization

    Write_Command(0x81);      // contrast control
    Write_Command(0x70);

    Write_Command(0xd5);      // display divide ratio/osc. freq. mode
    Write_Command(0x80);      // Osc. Freq:360kHz,DivideRation:1

    Write_Command(0xd9);      // set pre-charge period
    Write_Command(0x22);      // set period

    Write_Command(0xda);      // Set SEG Pins Hardware Configuration
    Write_Command(0x10);


    Write_Command(0xDB);      // VCOMH deselect level mode
    Write_Command(0x00);

    Write_Command(0xDC);    // Set VSL / GPIO
    Write_Command(0x01);    // enanble GPIO

    Write_Command(0x78);    // close SD
    Write_Command(0x38);
}
```

4.4 SSD1360Z CGROM Character Code

4.5.1 ROMA



4.5.2 RMOB


MSB
LSB
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
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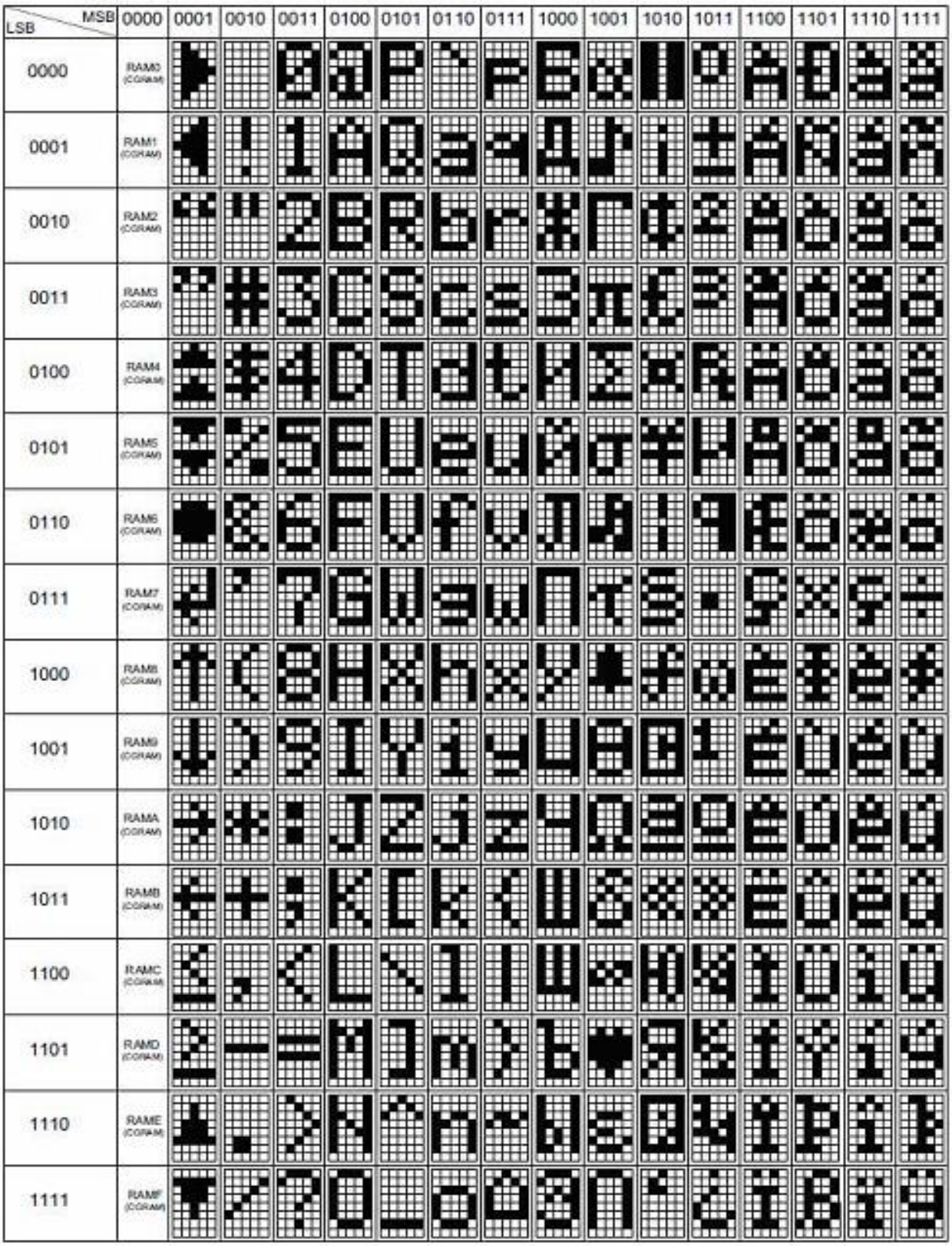
RAM1 (CGRAM)
RAM2 (CGRAM)
RAM3 (CGRAM)
RAM4 (CGRAM)
RAM5 (CGRAM)
RAM6 (CGRAM)
RAM7 (CGRAM)
RAM8 (CGRAM)
RAM9 (CGRAM)
RAMA (CGRAM)
RAMB (CGRAM)
RAMC (CGRAM)
RAMD (CGRAM)
RAME (CGRAM)
RAMF (CGRAM)

4.5.3 ROMC


MSB
LSB
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
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RAM1 (CGRAM)
RAM2 (CGRAM)
RAM3 (CGRAM)
RAM4 (CGRAM)
RAM5 (CGRAM)
RAM6 (CGRAM)
RAM7 (CGRAM)
RAM8 (CGRAM)
RAM9 (CGRAM)
RAMA (CGRAM)
RAMB (CGRAM)
RAMC (CGRAM)
RAMD (CGRAM)
RAME (CGRAM)
RAMF (CGRAM)

5. Relibality

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23+/−5℃； 55+/-15%RH。

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customers test & measurement are required to be conducted under the following conditions:

Temperature:	23+/−5℃
Humidity:	55+/−15%RH
Fluorescent Lamp:	30W
Distance between the Panel & Eyes of the Inspector :	⩾50cm
Finger glove (or finger cover) must be worn by the inspector.	⩾30cm

Inspection table or jig must be anti-electrostatic.

6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E