MOS FET

FJ3P02100L

Panasonic

FJ3P02100L

Silicon P-channel MOSFET

For Load-switching

■ Features

- Low drain-source ON resistance:RDS(on)typ. = $12.0 \text{m}\Omega$ (VGS = -2.5 V)
- · High heat dissipated and ultra-compact package PMCP
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)
- Marking Symbol: A0

■ Packaging

Embossed type (Thermo-compression sealing): 7 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

Parameter		Symbol	Rating	Unit	
Drain-source voltage		VDS	-20	V	
Gate-source voltage		VGS	±8	V	
Drain current	Ta = 25 °C, DC *2	ID1	-4.4	Α	
	Ta = 25 °C, DC *3	ID2	-7.5		
Drain current	Ta = 25 °C *1 *2	IDp1	-13.2	Α	
(Pulsed)	Ta = 25 °C *1 *3	IDp2	-22.5	ζ	
Total power	Ta = 25 °C, DC *2	PD1	300	mW	
dissipation	Ta = 25 °C, DC *3	PD2	850		
Channel tempe	erature	Tch	150	°C	
Storage temperature range		Tstg	-55 to +150	°C	

Note: *1 t = 10 μs, Duty Cycle < 1%

- *2 When mounted on glass epoxy board typeA (Refer to Figure1)
- *3 When mounted on glass epoxy board typeB (Refer to Figure2)

■ Electrical Characteristics Ta = 25 °C ±3 °C Static Characteristics

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source breakdown voltage	VDSS	ID = -1.0 mA, VGS = 0 V	-20			V
Zero gate voltage drain current	IDSS	VDS = -20 V, VGS = 0 V			-10	μA
Gate-source leakage current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate-source threshold voltage	Vth	ID = -1.0 mA, VDS = -10 V	-0.3	-0.65	-1.05	V
	RDS(on)1	ID = -3.7 A, VGS = -4.5 V		9.5	12.5	
Drain-source on-state resistance	RDS(on)2	ID = -3.7 A, VGS = -2.5 V		12.0	16.5	$m\Omega$
	RDS(on)3	ID = -3.7 A, VGS = -2.0 V		16.0	30.0	

Dynamicic Characteristics

Established: 2012-10-25

: 2013-02-05

Revised

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Input capacitance *1	Ciss			3000		
Output capacitance *1	Coss	VDS = -10 V, VGS = 0 V, f = 1 MHz		330		pF
Reverse transfer capacitance *1	Crss			350		

Package dimension Unit: mm

2.0

3

0.2

(0.25)

(0.8)

(0.8)

(0.8)

(0.8)

(0.8)

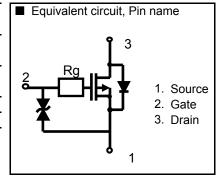
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1. Source
2. Gate

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Code

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Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Turn-on delay time *1 *2	td(on)	VDD = -10 V, VGS = 0 to -4 V,ID = -3.7 A		1		μs
Rise time *1 *2	tr			1.9		
Turn-off delay time *1 *2	td(off)	VDD = -10 V, VGS = -4 to 0 V,ID = -3.7 A		6.5		μs
Fall time *1 *2	tf	VDD = -10 V, VGS = -4 to 0 V,ID = -5.7 A		3.9		μδ

Note: 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

- 2. *1 Assured by design
 - *2 Refer to figure3, measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time

Figure1: Glass epoxy board typeA

Material:FR4, Size:25.4mm x 25.4mm x t 1.0mm, Cu pad:tickness 36 μm, 25.9mm²

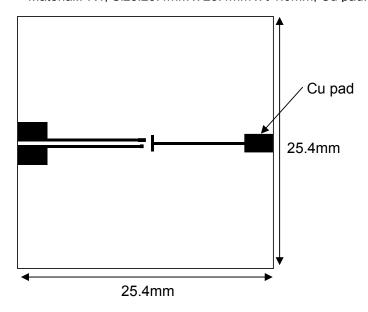
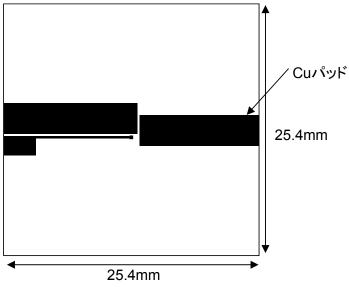


Figure2: Glass epoxy board typeB Material:FR4, Size:25.4mm x 25.4mm x t 1.0mm, Cu pad:tickness 36 μm, 82.0mm²



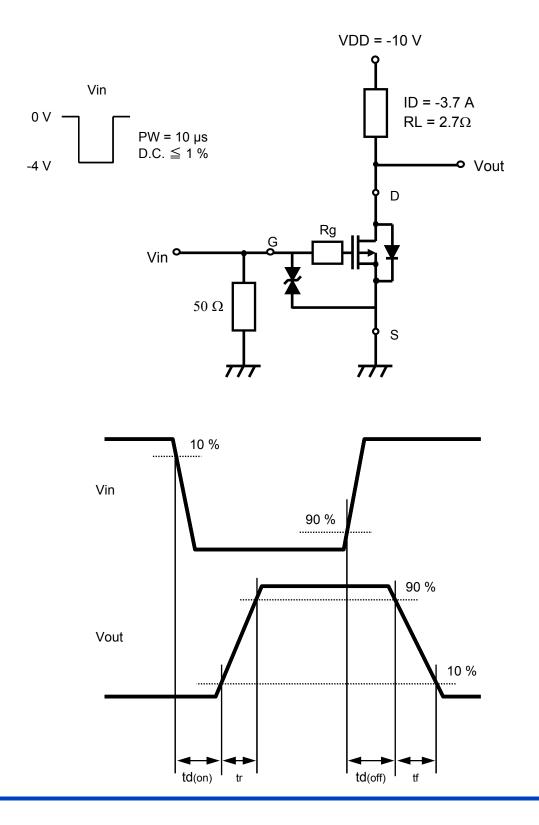
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Figure3: Measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time

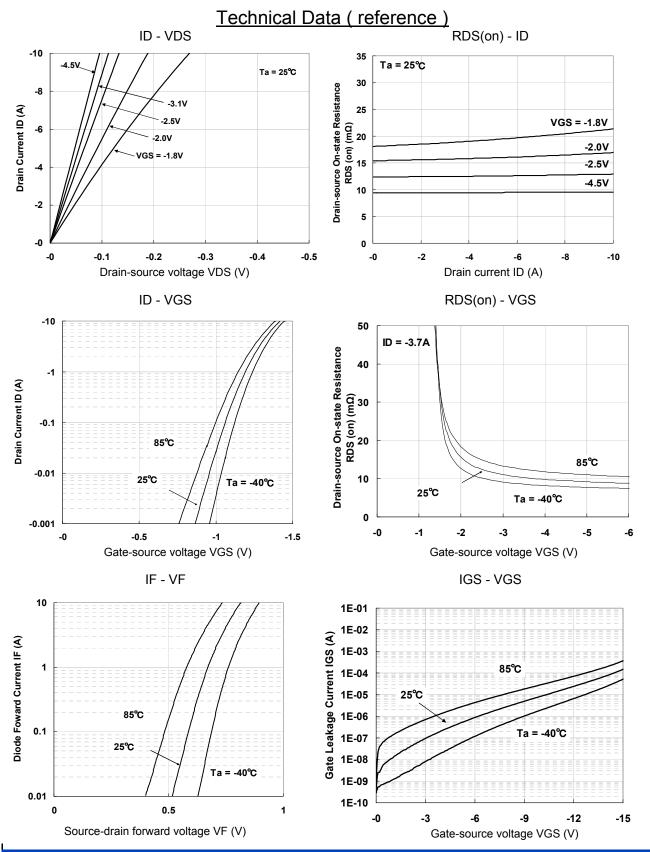


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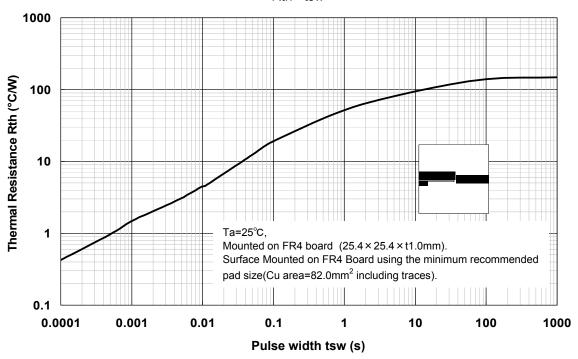


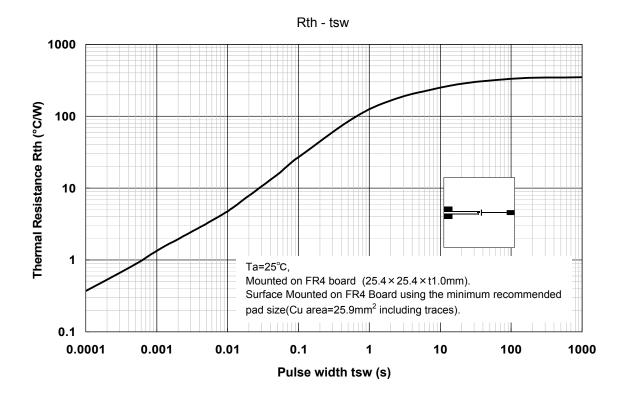
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<u>Technical Data (reference)</u> Rth - tsw





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Established: 2012-10-25 : 2013-02-05 Revised

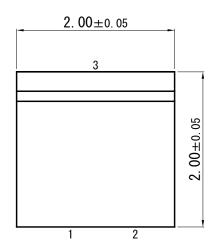
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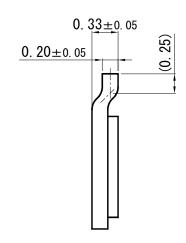
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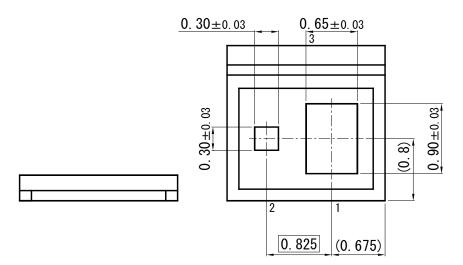
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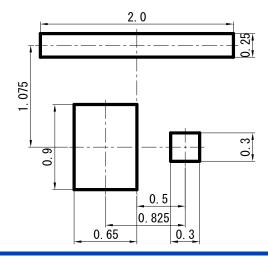
Unit: mm







■ Land Pattern (Reference) (Unit: mm)



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