Rockwell

PARALLEL PROCESSING SYSTEM (PPS)

DATA SHEET

GENERAL PURPOSE KEYBOARD AND DISPLAY CONTROL (GPKD)

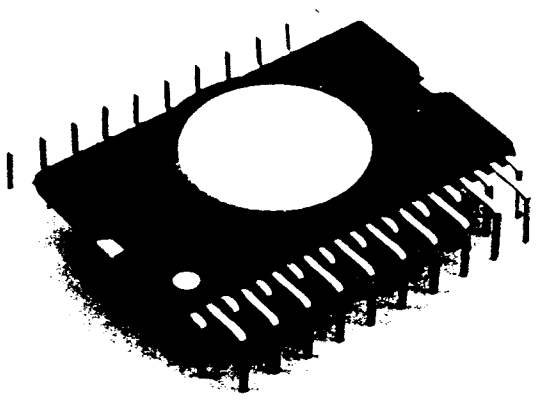
INTRODUCTION

This document describes General Purpose Keyboard and Display circuit P/N 10788, manufactured by the Microelectronic Device Division of Rockwell International. This versatile circuit provides the optimum method of interfacing the Rockwell Parallel Processing System (PPS) Microcomputers to a wide variety of keyboards and display devices. The General Purpose Keyboard and Display (GPKD) circuit interfaces the functional circuits in the PPS with the majority of business machine, Point-of-Sale (POS), and calculator keyboards and displays.

The General Purpose Keyboard and Display circuit (GPKD) connects directly with the PPS data bus. The GPKD is initialized by the Synchronized Power-On (SPO) signal from the CPU.

The keyboard controller functions of the GPKD strobe up to 64 single-pole, single-throw momentary switches on an 8 x 8 matrix and provide a 7.68 msec debounce delay for these switches. A 9-level, 8-bit key buffer allows up to nine key inputs to be stored until the PPS processes them. Inputs can be entered at an operating speed of 7.68 msec/character.

The display controller functions of the GPKD synchronize and strobe up to 16 characters of display data which are outputted in two hexadecimal groups. The two hexadecimal groups of data, designated as Group A and Group B, may be used as one group of 8-bit data or several groups of data composed of less than 8 bits. A typical application of the data display is to use 4 bits of data for numeric display, 2 bits for decimal point and comma, and the remaining 2 bits for display up to 32 status indicators. It is also possible to display 32 consecutive digits of numeric data and some symbols when two 16-digit hexadecimal groups are treated as one 32-digit hexadecimal code.



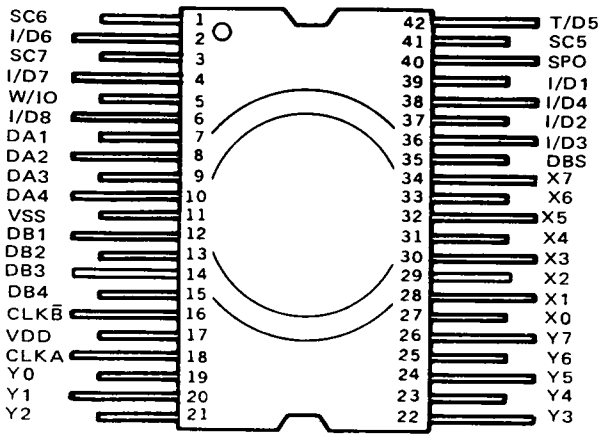
FEATURES

KEYBOARD

- Nine-Key Buffering
- Two-Key Rollover
- 7.68 msec Key Debounce Delay
- Handle up to 64 keys on 8 x 8 matrix
- Chip Address Strap Encoded
- Initialized at Power On (SPO)

DISPLAY

- Display up to 16 characters
- 32 Digits of Display Possible
- Two 16-Digit Display Buffers
- Two Sets of Hexadecimal Code Outputs for Display
- TTL Compatible Interface
- 5% Duty Cycle



GPKD Pin Configuration

Specifications subject to change without notice
Revision 1, March 1976

FUNCTIONAL DESCRIPTION

The GPKD block diagram shows the various functional circuits in the GPKD. The following paragraphs discuss the functional elements of the GPKD listed below:

- Chip Select Decode
- Command Decoding
- Bit Time Counter
- Scan Counter
- Display Register Control
- Display Register A
- Display Register B
- Display Bank Select
- Strobe Select
- Return Sampling
- Key Buffer Register Control
- Key Buffer Registers
- Key Code Transfer Control

CHIP SELECT DECODE

The chip select decode circuit compares the chip address data on data bus lines I/D5, I/D6, and I/D7 to the data on chip select straps SC5, SC6, and SC7. If the result is the same and the W/IO and I/D8 lines are true, the GPKD is selected.

COMMAND DECODING

The command decoding circuit determines which of the eight GPKD commands will be executed. The chip select decode logic enables the command decoding, which decodes the command inputs I/D1, I/D2, I/D3 and I/D4.

BIT TIME COUNTER

The bit time counter divides the PPS clock frequency by 8 to provide increment timing of the scan counter. One bit time equals one basic PPS cycle time, (typically 5 μsec).

SCAN COUNTER

The scan counter provides timing signals for the display register control, display bank select, return sampling, key buffer register control, and strobe select functions. The scan counter updates its count once every 8 bit times by using the bit time counter output.

The 8-bit codes generated by the scan counter represent corresponding keys on the key matrix. Upon a detection of a key depression, the scan counter content at that moment represents the depressed key and is transferred to the first key buffer register.

DISPLAY REGISTER CONTROL

The display register control logic controls load, shift hold, turn on, and turn off of display registers A and B. The scan counter provides the synchronizing signal to the display register control, and the command decoding function provides the signal that controls the modes of the display registers.

DISPLAY REGISTERS A AND B

Display registers A and B are used to store display data. Each display register consists of 16 4-bit storage registers. The contents of the storage registers can be changed only by I/O commands and, therefore, are independent of the system operations controlled by other than I/O commands. The display registers take the data from the data bus ID/5, ID/6, ID/7 and ID/8. Loading time and outputting of the display registers are controlled by display register control logic, which is governed by microprogrammed commands and the scan counter.

Each of the two display registers has four parallel open drain outputs each of which is capable of driving one TTL load. These outputs are synchronized with the strobe select lines and display bank select line. The outputs of display register A are designated DA1, DA2, DA3 and DA4, and the outputs of display register B are designated DB1, DB2, DB3 and DB4.

DISPLAY BANK SELECT

The display bank select combined with the eight strobe lines provides scanning for up to 16 characters of display. The display bank select output is designated as DBS. A VSS level on the DBS line selects the lower eight strobes and the VDD level on DBS selects the upper eight strobes, thus yielding a total of 16 strobes.

STROBE SELECT

The strobe select circuit sequentially outputs eight strobe signals designated X0 through X7, each on a separate output line. The first strobe occurs on X0, the second strobe occurs on X1, and strobes continue in sequence through X7, after which the strobes restart at X0. The strobes are used in forming an 8 by 8 XY keyboard matrix in which X corresponds to the strobe select lines and Y to the keyboard return lines. The strobe select, in conjunction with the display bank select, is also used for multiplexing up to 16 characters of display.

RETURN SAMPLING

The return sampling circuit tests the states of key matrix return lines from the keyboard. The results of the tests are used in the key buffer register control logic to determine the key status. The eight return lines from the keyboard XY matrix are designated Y0 through Y7.

KEY BUFFER REGISTER CONTROL

The key buffer register control performs the following two functions: (1) loads the key code generated by the scan counter into the first buffer register when the return sampling logic detects a key closure, and (2) controls the "first in, first out" operation of the key buffer registers.

KEY BUFFER REGISTERS

The GPKD has nine 8-bit key buffer registers to store key codes (keyboard entries) until transferred out by PPS request. Upon a key closure detection, the corresponding code generated by the scan counter is loaded into the first key buffer register, then transferred to the next key buffer register if it is empty. If all nine buffer registers are full and another key is depressed the MSB of the ninth key code goes from 0 to 1. A "1" in the MSB indicates to the CPU that the key buffer register storage capacity has been exceeded, and that one or more key entries may have been lost. The CPU will reset this error condition using the KER instruction. The data in the first eight buffer registers will be accepted by the CPU as valid data.

KEY CODE TRANSFER CONTROL

The key code transfer control outputs data from the last key buffer register to the I/D bus upon request by the PPS CPU. The output of data is handled on a "first in, first out" basis.

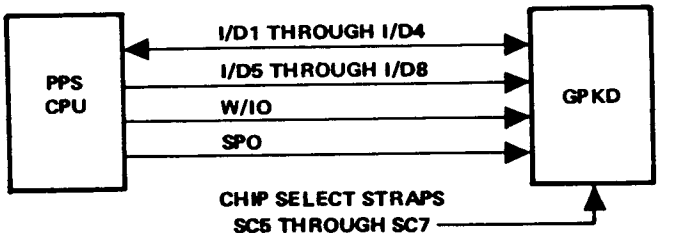
INTERFACE

The interface considerations of the GPKD are divided into three functions for explanation purposes. These functions are as follows:

PPS CPU Interface to GPKD
Keyboard Interface to GPKD
Display Interface to GPKD

PPS CPU INTERFACE TO THE GPKD

Physical interconnection of the CPU to the GPKD is accomplished by connecting CPU lines to GPKD circuit pins of the same designation. The interface is shown in the figure below. CPU lines connected to the GPKD are I/D1 - I/D8, SPO, and W/IO.

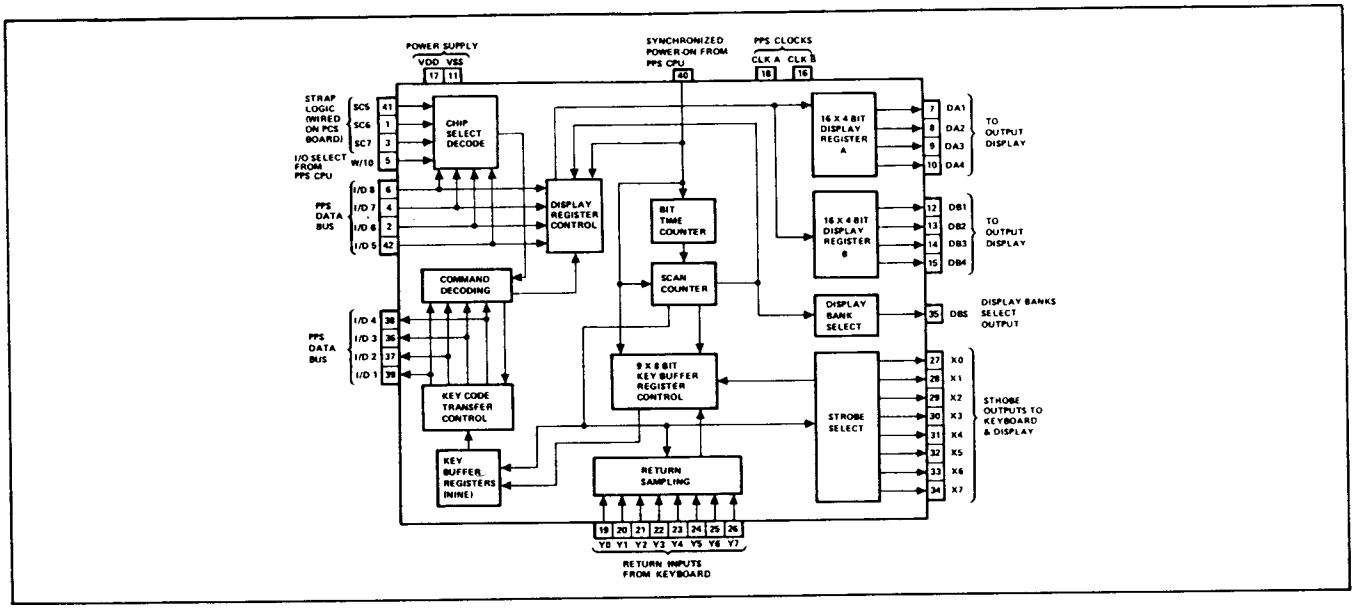


KEYBOARD INTERFACE TO GPKD

The GPKD has 16 lines which form a keyboard matrix. Eight of the lines are strobe lines designated X0 through X7 and the other eight lines are return lines designated Y0 through Y7. Two IOL instructions are required to read in a designated key location, one instruction for strobe line data and the other instruction for return line data.

DISPLAY INERFACE TO GPKD

Two groups of four 16-bit registers are used to store display data. Each of these two register groups has four outputs and each output is capable of driving one TTL load. The GPKD is designed to use TTL logic to interface to the many different commercial displays.



GPKD Block Diagram

SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:

VDD = -17 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)

VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies:

199 kHz or 256 kHz.

Device Power Consumption:

200 mw

Input Capacitance:

<5 pf

Input Leakage:

<10 ua

Operating Temperature (TA):

0°C to 70°C. (TA = 25°C unless otherwise specified.)

Storage Temperature:

-55°C to 120°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

|VDD-VSS| = 27 volts maximum.

Input Voltage with respect to VSS
-27 volts maximum.

Maximum positive voltage on any pin +0.3 volts.

FUNCTION		SYMBOL	LIMITS (VSS = 0V) MIN	TYP	MAX	LIMITS (VSS = +5V) MIN	TYP	MAX	UNIT	TEST CONDITIONS
Supply Current (Average)		I_{DD}		4	11		4	11	mA	VDD = -17.85V VSS = 0V F = 256 kHz T_A = 25°C
Input and Output Characteristics — System Bus										VDD = -17V ±5% VSS = 0V
I/D_{1-4}	I/D_{5-8} W/IO	V_{IH} V_{IL}	-1.5 -6.5		+0.3 -17.85	+3.5 -1.5		+5.3 -12.85	V V	
		V_{OH} V_{OL}	-1.0 -7.5		+0.3 -17.85	+4.0 -2.5		+5.3 -12.85	V V	
SC_{5-7}		V_{IH} V_{IL}	-1.5 -13.0		+5.3 -17.85	+3.5 -8.0		+5.3 -12.85	V V	
SPO		V_{IH} V_{IL}	-1.0 -7.5		+0.3 -17.85	+4.0 -2.5		+5.3 -12.85	V V	OR
CLKA CLKB		V_{IH} V_{IL}	-0.5 -10.0		+0.3 -17.85	+4.5 -5.0		+5.3 -12.85	V V	
Input and Output Characteristics — External Interface										
Y_{0-7}		V_{IH} V_{IL}	-4.0 -13.0		+0.3 -17.85	+1.0 -8.0		+5.3 -12.85	V V	
X_{0-7}, DA_{1-4}, DB_{1-4}, DBS		V_{OH} V_{OL}	NOTE 1 floating (≥5M)			NOTE 1 floating (≥5M)			Ω	VDD = -12V ±5% VSS = +5V ±5%

NOTE: 1. Output driven to VSS with maximum "ON" resistance (RON_{MAX}) of 1.0K ohms and maximum current (I_{MAX}) of 2.7 ma.

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