

MC74HCT573A

Octal 3-State Noninverting Transparent Latch with LSTTL Compatible Inputs High-Performance Silicon-Gate CMOS

The MC74HCT573A is identical in pinout to the LS573. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

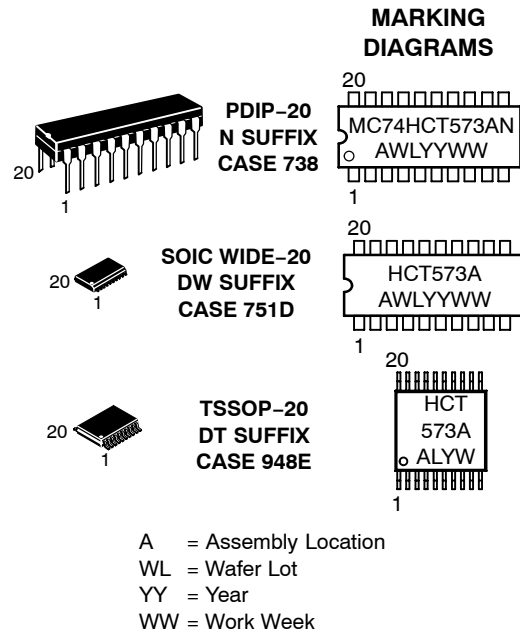
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT573A is identical in function to the HCT373A but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 10 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
 - Improved Propagation Delays
 - 50% Lower Quiescent Power
- These devices are available in Pb-free package(s). Specifications herein apply to both standard and Pb-free devices.



ON Semiconductor



ORDERING INFORMATION

Device	Package	Shipping
MC74HCT573AN	PDIP-20	1440 / Box
MC74HCT573ADW	SOIC-WIDE	38 / Rail
MC74HCT573ADWR2	SOIC-WIDE	1000 / Reel
MC74HCT573ADT	TSSOP-20	75 / Rail
MC74HCT573ADTR2	TSSOP-20	2500 / Reel

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air	750	mW
	Plastic DIP†	500	
	SOIC Package† TSSOP Package†	450	
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, TSSOP or SOIC Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C
TSSOP Package: -6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	- 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	4.5	0.1	1.0	1.0	μA
			5.5	± 0.1	± 1.0	± 1.0	
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or } GND$	5.5	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} \leq 0 \mu\text{A}$	5.5	4.0	40	160	μA
			5.5	2.9	2.4	2.4	
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or } GND, \text{ Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ - 55°C	25°C to 125°C		mA
				2.9	2.4		

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V} \pm 10\%$, $C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		- 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input D to Output Q (Figures 1 and 5)	30	38	45	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	30	38	45	ns
T_{PLZ} , T_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t_{TZL} , t_{TZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	28	35	42	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, any Output (Figures 1 and 5)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$		pF
		48		

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

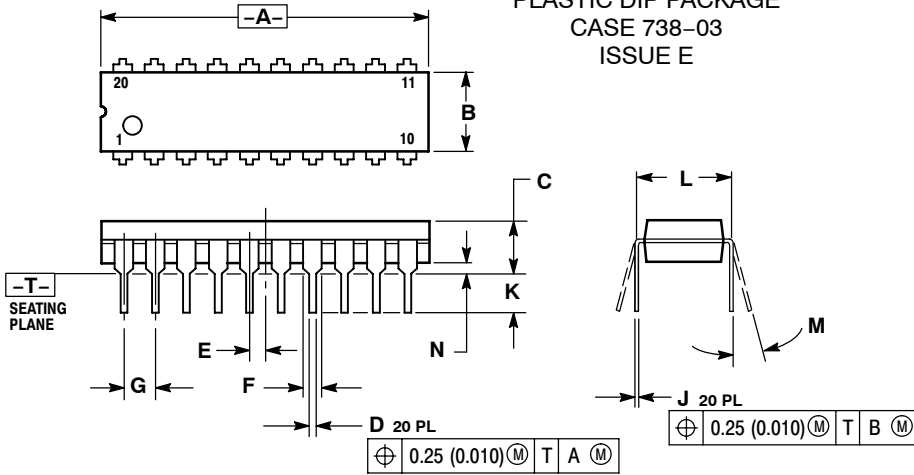
TIMING REQUIREMENTS ($V_{CC} = 5.0\text{ V} \pm 10\%$, $C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			- 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Input D to Latch Enable	4	10		13		15		ns
t_h	Minimum Hold Time, Latch Enable to Input D	4	5.0		5.0		5.0		ns
t_w	Minimum Pulse Width, Latch Enable	2	15		19		22		ns
t_r, t_f	Maximum Input Rise and Fall Times	1		500		500		500	ns

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PACKAGE DIMENSIONS

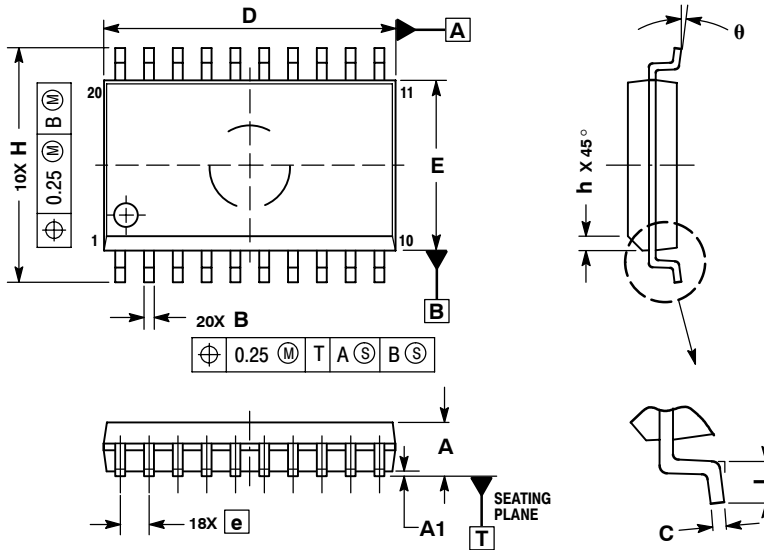
PDIP-20
N SUFFIX
 PLASTIC DIP PACKAGE
 CASE 738-03
 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO-20
DW SUFFIX
 CASE 751D-05
 ISSUE F



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°