

MC100EP016A

3.3 V ECL 8-Bit Synchronous Binary Up Counter

Description

The MC100EP016A is a high-speed synchronous, presettable, cascadeable 8-bit binary counter. Architecture and operation are the same as the ECLinPS™ family MC100E016 with higher operating speed.

The counter features internal feedback to \overline{TC} gated by the TCLD (Terminal Count Load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pulldowns), the \overline{TC} feedback is disabled, and counting proceeds continuously, with \overline{TC} going LOW to indicate an all-one state. When TCLD is HIGH, the TC feedback causes the counter to automatically reload upon $TC = LOW$, thus functioning as a programmable counter. The Qn outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated.

COUT and \overline{COUT} provide differential outputs from a single, non-cascaded counter or divider application. COUT and \overline{COUT} should not be used in cascade configuration. Only \overline{TC} should be used for a counter or divider cascade chain output.

A differential clock input has also been added to improve performance.

The 100 Series contains temperature compensation.

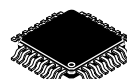
Features

- 550 ps Typical Propagation Delay
- Operation Frequency > 1.3 GHz is 30% Faster than MC100EP016
- PECL Mode Operating Range: $V_{CC} = 3.0\text{ V}$ to 3.6 V with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -3.0\text{ V}$ to -3.6 V
- Open Input Default State
- Safety Clamp on Clock Inputs
- Internal \overline{TC} Feedback (Gated)
- Addition of COUT and \overline{COUT}
- 8-Bit
- Differential Clock Input
- V_{BB} Output
- Fully Synchronous Counting and \overline{TC} Generation
- Asynchronous Master Reset
- Pb-Free Packages are Available

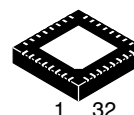
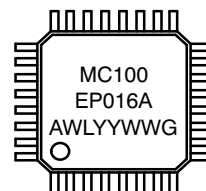


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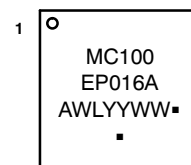
MARKING DIAGRAMS*



LQFP-32
FA SUFFIX
CASE 873A



QFN32
MN SUFFIX
CASE 488AM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

MC100EP016A

Table 4. ATTRIBUTES

Characteristics	Value	
Internal Input Pulldown Resistor	75 kΩ	
Internal Input Pullup Resistor	N/A	
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 100 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
	LQFP-32	Level 2
	QFN-32	Level 2 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count	1226 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-6	V
V _I	PECL Mode Input Voltage	V _{EE} = 0 V	V _I ≤ V _{CC}	6	V
	NECL Mode Input Voltage	V _{CC} = 0 V	V _I ≥ V _{EE}	-6	V
I _{out}	Output Current	Continuous		50	mA
		Surge		100	mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			-40 to +70	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm	32 LQFP	74	°C/W
		500 lfpm	32 LQFP	61	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	32 LQFP	12 to 17	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm	QFN-32	31	°C/W
		500 lfpm	QFN-32	27	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	2S2P	QFN-32	12	°C/W
T _{sol}	Wave Solder	Pb		265	°C
		Pb-Free		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

MC100EP016A

Table 6. 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 2)

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	130	170	210	130	177	210	130	180	210	mA
V_{OH}	Output HIGH Voltage (Note 3)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -0.3 V.

3. All loading with 50 ohms to V_{CC} -2.0 volts.

4. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.6\text{ V}$ to -3.0 V (Note 5)

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	130	170	210	130	177	210	130	180	210	mA
V_{OH}	Output HIGH Voltage (Note 6)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 6)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{BB}	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC} .

6. All loading with 50 ohms to V_{CC} -2.0 volts.

7. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC100EP016A

Table 8. AC CHARACTERISTICS $V_{EE} = -3.0\text{ V to }-3.6\text{ V}$; $V_{CC} = 0\text{ V or }3.0\text{ V to }3.6\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 8)

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{COUNT}	Maximum Frequency Count & Division Modes Q, $\overline{\text{TC}}$, $\text{COUT}/\overline{\text{COUT}}$	1.3	1.5		1.2	1.4		1.2	1.3		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q MR to Q CLK to $\overline{\text{TC}}$ MR to $\overline{\text{TC}}$ CLK to $\text{COUT}/\overline{\text{COUT}}$ MR to $\text{COUT}/\overline{\text{COUT}}$	350 400 350 400 475 450	511 550 511 555 705 720	650 700 650 700 850 850	400 400 400 400 500 500	550 570 550 570 745 760	700 750 700 750 900 900	480 450 480 520 550 570	610 630 610 635 825 830	780 820 780 820 1000 950	ps
t_{S}	Setup Time P0 P1 to P4 P5 to P7 $\overline{\text{CE}}$ $\overline{\text{PE}}$ TCLD	400 300 250 500 500 550	240 140 80 320 315 355		400 300 250 500 500 550	240 135 65 330 320 365		400 300 250 500 500 550	245 125 55 340 325 380		ps
t_{H}	Hold Time P0 P1 to P4 P5 to P7 $\overline{\text{CE}}$ $\overline{\text{PE}}$ TCLD	100 50 150 600 625 525	-145 -160 -105 380 465 320		100 50 150 600 625 525	-155 -170 -110 410 500 325		100 50 150 600 625 525	-170 -180 -115 450 535 340		ps
t_{JITTER}	Clock Random Jitter (RMS, 1000 Waveforms)		2.6	8.5		2.5	8.0		2.5	8.0	ps
t_{RR}	Reset Recovery Time	400	195		400	205		400	220		ps
t_{PW}	Minimum Pulse Width CLK Minimum Pulse Width MR	385 550	334 380		416 550	357 380		416 550	385 380		ps
$t_{\text{r}}, t_{\text{f}}$	Output Rise/Fall Times 20% - 80%	90	180	320	100	190	320	125	215	450	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to $V_{CC}-2.0\text{ V}$.

MC100EP016A

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP016AFA	LQFP-32	250 Units / Tray
MC100EP016AFAG	LQFP-32 (Pb-Free)	250 Units / Tray
MC100EP016AFAR2	LQFP-32	2000 / Tape & Reel
MC100EP016AFAR2G	LQFP-32 (Pb-Free)	2000 / Tape & Reel
MC100EP016AMNG	QFN-32 (Pb-Free)	74 Units / Rail
MC100EP016AMNR4G	QFN-32 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

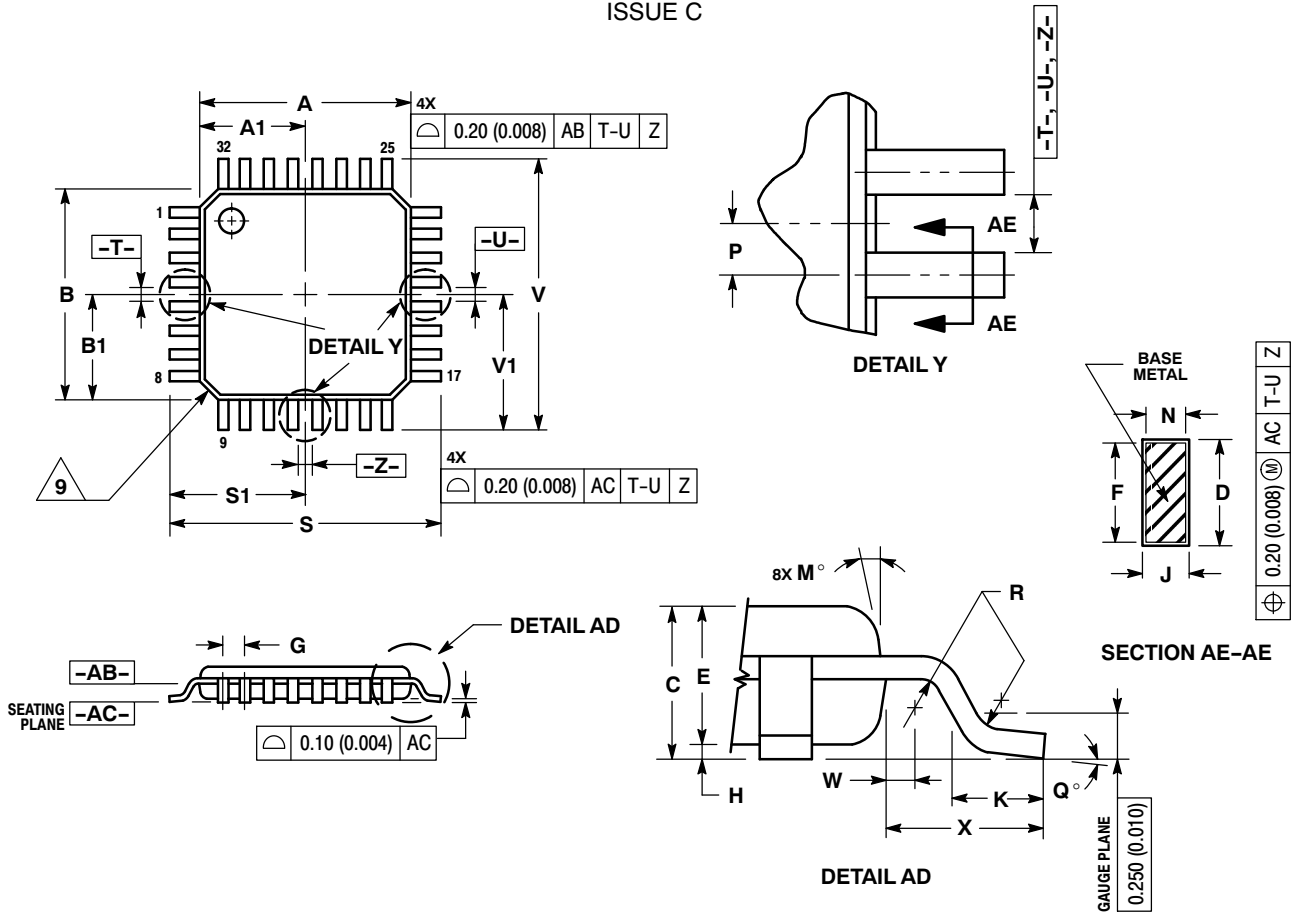
Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices

MC100EP016A

PACKAGE DIMENSIONS

32 LEAD LQFP
CASE 873A-02
ISSUE C



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
- DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
- MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
- EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000	BSC	0.276	BSC
A1	3.500	BSC	0.138	BSC
B	7.000	BSC	0.276	BSC
B1	3.500	BSC	0.138	BSC
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800	BSC	0.031	BSC
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.750	0.018	0.030
M	12°	REF	12°	REF
N	0.090	0.160	0.004	0.006
P	0.400	BSC	0.016	BSC
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000	BSC	0.354	BSC
S1	4.500	BSC	0.177	BSC
V	9.000	BSC	0.354	BSC
V1	4.500	BSC	0.177	BSC
W	0.200	REF	0.008	REF
X	1.000	REF	0.039	REF