MC74VHC1GT14

Schmitt-Trigger Inverter / CMOS Logic Level Shifter

LSTTL−Compatible Inputs

The MC74VHC1GT14 is a single gate CMOS Schmitt−trigger inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL−type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic−level translator from 3 V CMOS logic to 5 V CMOS Logic or from 1.8 V CMOS logic to 3 V CMOS Logic while operating at the high−voltage power supply.

The MC74VHC1GT14 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT14 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when V_{CC} = 0 V. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc. The MC74VHC1GT14 can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- High Speed: t_{PD} = 4.5 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2 V
- CMOS−Compatible Outputs: V_{OH} > 0.8 V_{CC}; V_{OL} < 0.1 V_{CC} @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 100; Equivalent Gates = 25
- Pb−Free Packages are Available

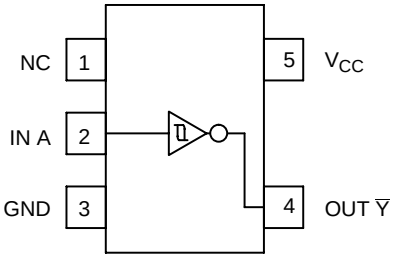


Figure 1. Pinout (Top View)

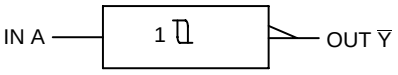
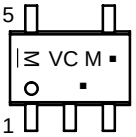


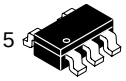
Figure 2. Logic Symbol

ON Semiconductor®

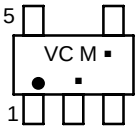
MARKING DIAGRAMS

SC−88A/SC70−5/SOT−353
DF SUFFIX
CASE 419A





TSOP−5/SOT23−5/SC59−5
DT SUFFIX
CASE 483



VC = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

1	NC
2	IN A
3	GND
4	OUT $\overline{Y}$
5	V_{CC}

FUNCTION TABLE

A Input	$\overline{Y}$ Output
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

Publication Order Number:
MC74VHC1GT14/D

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage	V_{CC} = 0 High or Low State	−0.5 to 7.0 −0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	+20	mA
I_{OUT}	DC Output Current, per Pin		+25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+50	mA
P_D	Power Dissipation in Still Air	SC−88A, TSOP−5	200	mW
θ_{JA}	Thermal Resistance	SC−88A, TSOP−5	333	°C/W
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
T_{stg}	Storage Temperature		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 N/A	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 4)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		3.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage	V_{CC} = 0 High or Low State	0.0 0.0	5.5 V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	− −	No Limit No Limit	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

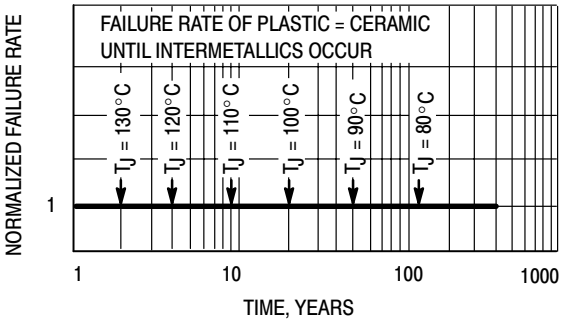


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55 \le T_A \le 125°C$ Min	$-55 \le T_A \le 125°C$ Max	Unit
V_{T+}	Positive Threshold Voltage		3.0 4.5 5.5	1.20 1.58 1.79	1.40 1.74 1.94	1.60 2.00 2.10		1.6 2.0 2.0		1.6 2.0 2.0	V
V_{T-}	Negative Threshold Voltage		3.0 4.5 5.5	0.35 0.5 0.6	0.76 1.01 1.13	0.93 1.18 1.29	0.35 0.5 0.6		0.35 0.5 0.6		V
V_H	Hysteresis Voltage		3.0 4.5 5.5	0.30 0.40 0.50	0.64 0.73 0.81	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V_{OH}	Minimum High−Level Output Voltage	$V_{IN} \le V_T$ − Min I_{OH} = −50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low−Level Output Voltage	$V_{IN} \ge V_T$ + Max I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r/t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55 \le T_A \le 125°C$ Min	$-55 \le T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to $\overline{Y}$	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF C_L = 50 pF		7.0 8.4	12.8 16.3	1.0 1.0	15.0 18.5	1.0 1.0	17.0 20.5	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		4.5 5.8	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	11.5 13.5	
C_{IN}	Maximum Input Capacitance			5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 5)	10	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

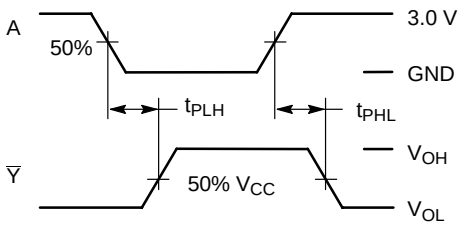
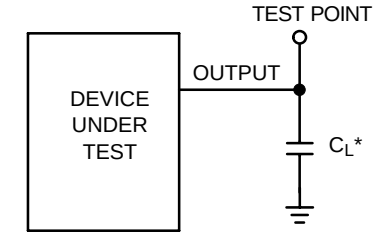


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

Figure 5. Test Circuit

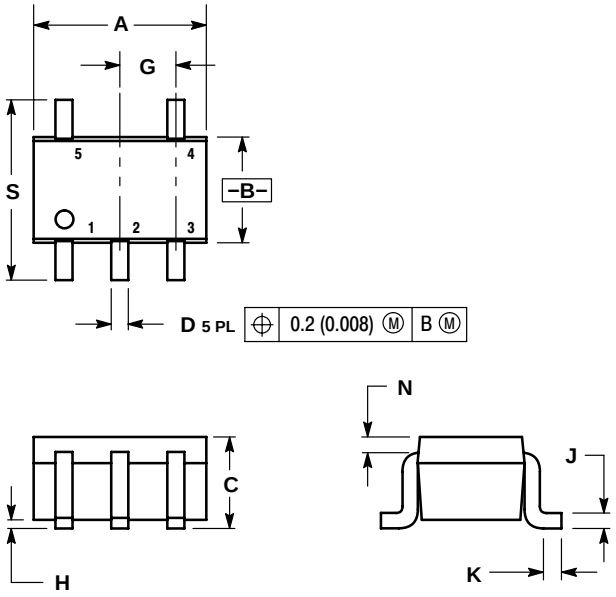
ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC1GT14DFT1	SC70−5/SC−88A/SOT−353	3000/Tape & Reel
M74VHC1GT14DFT1G	SC70−5/SC−88A/SOT−353 (Pb−Free)	
MC74VHC1GT14DFT2	SC70−5/SC−88A/SOT−353	
M74VHC1GT14DFT2G	SC70−5/SC−88A/SOT−353 (Pb−Free)	
MC74VHC1GT14DTT1	SOT23−5/TSOP−5/SC59−5	
M74VHC1GT14DTT1G	SOT23−5/TSOP−5/SC59−5 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

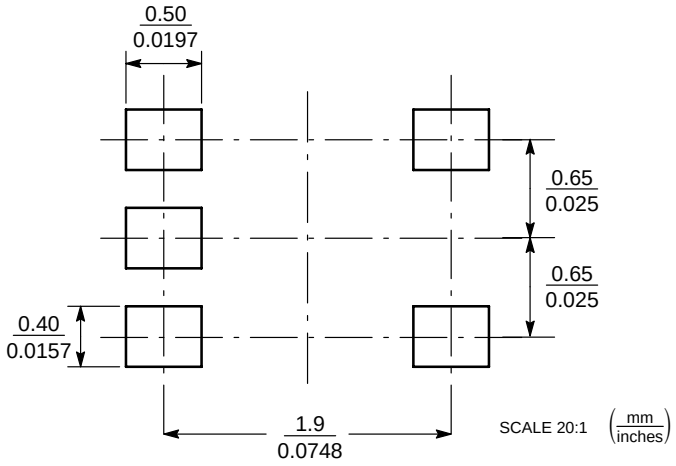
SC−88A, SOT−353, SC−70
CASE 419A−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.