LP2950, LP2951, NCV2951

100 mA, Low Power Low Dropout Voltage Regulator

The LP2950 and LP2951 are micropower voltage regulators that are specifically designed to maintain proper regulation with an extremely low input−to−output voltage differential. These devices feature a very low quiescent bias current of 75 μA and are capable of supplying output currents in excess of 100 mA. Internal current and thermal limiting protection is provided.

The LP2951 has three additional features. The first is the $\overline{\text{Error}}$ Output that can be used to signal external circuitry of an out of regulation condition, or as a microprocessor power−on reset. The second feature allows the output voltage to be preset to 5.0 V, 3.3 V or 3.0 V output (depending on the version) or programmed from 1.25 V to 29 V. It consists of a pinned out resistor divider along with direct access to the Error Amplifier feedback input. The third feature is a Shutdown input that allows a logic level signal to turn−off or turn−on the regulator output.

Due to the low input−to−output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable. The LP2950 is available in the three pin case 29 and DPAK packages, and the LP2951 is available in the eight pin dual−in−line, SOIC−8 and Micro8 surface mount packages. The 'A' suffix devices feature an initial output voltage tolerance ±0.5%.

Features

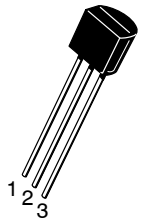
- Low Quiescent Bias Current of 75 μA
- Low Input−to−Output Voltage Differential of 50 mV at 100 μA and 380 mV at 100 mA
- 5.0 V, 3.3 V or 3.0 V ±0.5% Allows Use as a Regulator or Reference
- Extremely Tight Line and Load Regulation
- Requires Only a 1.0 μF Output Capacitor for Stability
- Internal Current and Thermal Limiting
- Pb−Free Packages are Available
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes

LP2951 Additional Features

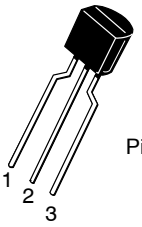
- $\overline{\text{Error}}$ Output Signals an Out of Regulation Condition
- Output Programmable from 1.25 V to 29 V
- Logic Level Shutdown Input

(See Following Page for Device Information.)

ON Semiconductor®



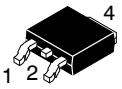
STRAIGHT LEAD
BULK PACK



BENT LEAD
TAPE & REEL
AMMO PACK

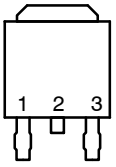
TO−92
Z SUFFIX
CASE 29

Pin: 1. Output
2. Ground
3. Input



DPAK
DT SUFFIX
CASE 369C

PIN CONNECTIONS



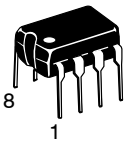
(Top View)

Pin: 1. Input
2. Ground
3. Output

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

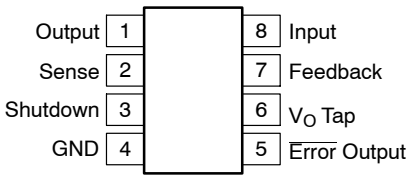
SOIC−8
D SUFFIX
CASE 751

PDIP−8
N SUFFIX
CASE 626



Micro8™
DM SUFFIX
CASE 846A

PIN CONNECTIONS



(Top View)

ORDERING & MARKING INFORMATION

See detailed ordering and shipping information in the package dimensions section on pages 14 and 16 of this data sheet. See general marking information in the device marking section on page 18 of this data sheet.

Publication Order Number:
LP2950/D

DEVICE INFORMATION

Package	Output Voltage				Operating Ambient Temperature Range
	3.0 V	3.3 V	5.0 V	Adjustable	
TO−92 Suffix Z	LP2950CZ−3.0 LP2950ACZ−3.0	LP2950CZ−3.3 LP2950ACZ−3.3	LP2950CZ−5.0 LP2950ACZ−5.0	Not Available	T_A = −40° to +125°C
DPAK Suffix DT	LP2950CDT−3.0 LP2950ACDT−3.0	LP2950CDT−3.3 LP2950ACDT−3.3	LP2950CDT−5.0 LP2950ACDT−5.0	Not Available	T_A = −40° to +125°C
SOIC−8	−	NCV2951ACD−3.3R2	NCV2951ACDR2	NCV2951CDR2	T_A = −40° to +125°C
SOIC−8 Suffix D	LP2951CD−3.0 LP2951ACD−3.0	LP2951CD−3.3 LP2951ACD−3.3	LP2951CD LP2951ACD	LP2951CD LP2951ACD	T_A = −40° to +125°C
Micro8 Suffix DM	LP2951CDM−3.0 LP2951ACDM−3.0	LP2951CDM−3.3 LP2951ACDM−3.3	LP2951CDM LP2951ACDM	LP2951CDM LP2951ACDM	T_A = −40° to +125°C
DIP−8 Suffix N	LP2951CN−3.0 LP2951ACN−3.0	LP2951CN−3.3 LP2951ACN−3.3	LP2951CN LP2951ACN	LP2951CN LP2951ACN	T_A = −40° to +125°C

LP2950Cx−xx / LP2951Cxx−xx 1% Output Voltage Precision at T_A = 25°C
LP2950ACx−xx / LP2951ACxx−xx 0.5% Output Voltage Precision at T_A = 25°C

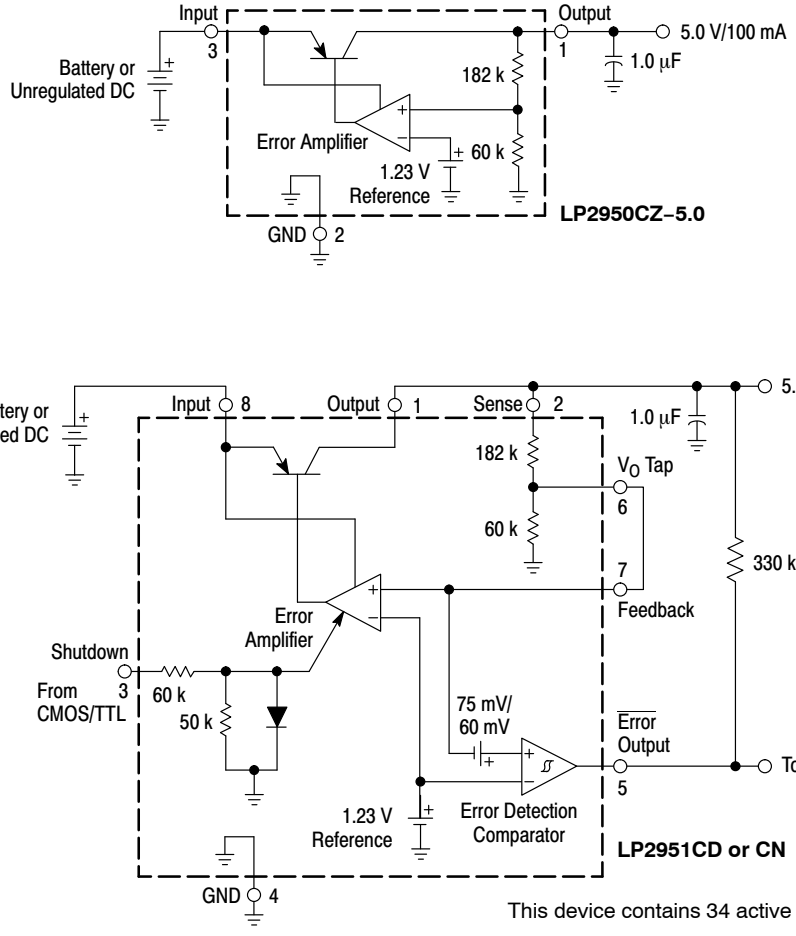


Figure 1. Representative Block Diagrams

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_{CC}	30	Vdc
Peak Transient Input Voltage (t < 20 ms)	V_{CC}	32	Vdc
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation	P_D	Internally Limited	W
Case 751(SOIC−8) D Suffix			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	180	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	45	°C/W
Case 369A (DPAK) DT Suffix (Note 1)			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	92	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.0	°C/W
Case 29 (TO−226AA/TO−92) Z Suffix			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	160	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83	°C/W
Case 626 N Suffix			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	105	°C/W
Case 846A (Micro8) DM Suffix			
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	240	°C/W
Feedback Input Voltage	V_{fb}	−1.5 to +30	Vdc
Shutdown Input Voltage	V_{sd}	−0.3 to +30	Vdc
Error Comparator Output Voltage	V_{err}	−0.3 to +30	Vdc
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Maximum Die Junction Temperature Range	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{in} = V_O + 1.0 V, I_O = 100 μA, C_O = 1.0 μF, T_A = 25°C [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage, 5.0 V Versions	V_O				V
V_{in} = 6.0 V, I_O = 100 μA, T_A = 25°C					
LP2950C−5.0/LP2951C/NCV2951C*		4.950	5.000	5.050	
LP2950AC−5.0/LP2951AC/NCV2951AC*		4.975	5.000	5.025	
T_A = −40 to +125°C					
LP2950C−5.0/LP2951C/NCV2951C*		4.900	–	5.100	
LP2950AC−5.0/LP2951AC/NCV2951AC*		4.940	–	5.060	
V_{in} = 6.0 to 30 V, I_O = 100 μA to 100 mA, T_A = −40 to +125°C					
LP2950C−5.0/LP2951C/NCV2951C*		4.880	–	5.120	
LP2950AC−5.0/LP2951AC/NCV2951AC*		4.925	–	5.075	
Output Voltage, 3.3 V Versions	V_O				V
V_{in} = 4.3 V, I_O = 100 μA, T_A = 25°C					
LP2950C−3.3/LP2951C−3.3		3.267	3.300	3.333	
LP2950AC−3.3/LP2951AC−3.3/NCV2951AC−3.3*		3.284	3.300	3.317	
T_A = −40 to +125°C					
LP2950C−3.3/LP2951C−3.3		3.234	–	3.366	
LP2950AC−3.3/LP2951AC−3.3/NCV2951AC−3.3*		3.260	–	3.340	
V_{in} = 4.3 to 30 V, I_O = 100 μA to 100 mA, T_A = −40 to +125°C					
LP2950C−3.3/LP2951C−3.3		3.221	–	3.379	
LP2950AC−3.3/LP2951AC−3.3/NCV2951AC−3.3*		3.254	–	3.346	
Output Voltage, 3.0 V Versions	V_O				V
V_{in} = 4.0 V, I_O = 100 μA, T_A = 25°C					
LP2950C−3.0/LP2951C−3.0		2.970	3.000	3.030	
LP2950AC−3.0/LP2951AC−3.0		2.985	3.000	3.015	
T_A = −40 to +125°C					
LP2950C−3.0/LP2951C−3.0		2.940	–	3.060	
LP2950AC−3.0/LP2951AC−3.0		2.964	–	3.036	
V_{in} = 4.0 to 30 V, I_O = 100 μA to 100 mA, T_A = −40 to +125°C					
LP2950C−3.0/LP2951C−3.0		2.928	–	3.072	
LP2950AC−3.0/LP2951AC−3.0		2.958	–	3.042	

1. The Junction−to−Ambient Thermal Resistance is determined by PCB copper area per Figure 29.
2. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM), 2000 V, Class 2, JESD22 A114−C
   Machine Model (MM), 200 V, Class B, JESD22 A115−A
   Charged Device Model (CDM), 2000 V, Class IV, JESD22 C101−C
3. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. $V_{O(nom)}$ is the part number voltage option.
5. Noise tests on the LP2951 are made with a 0.01 μF capacitor connected across Pins 7 and 1.

*NCV prefix is for automotive and other applications requiring site and change control.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = V_O + 1.0 V, I_O = 100 μA, C_O = 1.0 μF, T_A = 25°C [Note 8], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Line Regulation (V_{in} = $V_{O(nom)}$ +1.0 V to 30 V) (Note 9)	Reg_{line}				%
LP2950C−XX/LP2951C/LP2951C−XX/NCV2951C*		−	0.08	0.20	
LP2950AC−XX/LP2951AC/LP2951AC−XX/NCV2951AC*		−	0.04	0.10	
Load Regulation (I_O = 100 μA to 100 mA)	Reg_{load}				%
LP2950C−XX/LP2951C/LP2951C−XX/NCV2951C*		−	0.13	0.20	
LP2950AC−XX/LP2951AC/LP2951AC−XX/NCV2951AC*		−	0.05	0.10	
Dropout Voltage	$V_I - V_O$				mV
I_O = 100 μA		−	30	80	
I_O = 100 mA		−	350	450	
Supply Bias Current	I_{CC}				
I_O = 100 μA		−	93	120	μA
I_O = 100 mA		−	4.0	12	mA
Dropout Supply Bias Current (V_{in} = $V_{O(nom)}$ − 0.5 V, I_O = 100 μA) (Note 9)	$I_{CCdropout}$	−	110	170	μA
Current Limit (V_O Shorted to Ground)	I_{Limit}	−	220	300	mA
Thermal Regulation	$Reg_{thermal}$	−	0.05	0.20	%/W
Output Noise Voltage (10 Hz to 100 kHz) (Note 10)	V_n				μVrms
C_L = 1.0 μF		−	126	−	
C_L = 100 μF		−	56	−	
LP2951A/LP2951AC Only					
Reference Voltage (T_A = 25°C)	V_{ref}				V
LP2951C/LP2951C−XX/NCV2951C*		1.210	1.235	1.260	
LP2951AC/LP2951AC−XX/NCV2951AC*		1.220	1.235	1.250	
Reference Voltage (T_A = −40 to +125°C)	V_{ref}				V
LP2951C/LP2951C−XX/NCV2951C*		1.200	−	1.270	
LP2951AC/LP2951AC−XX/NCV2951AC*		1.200	−	1.260	
Reference Voltage (T_A = −40 to +125°C)	V_{ref}				V
I_O = 100 μA to 100 mA, V_{in} = 23 to 30 V					
LP2951C/LP2951C−XX/NCV2951C*		1.185	−	1.285	
LP2951AC/LP2951AC−XX/NCV2951AC*		1.190	−	1.270	
Feedback Pin Bias Current	I_{FB}	−	15	40	nA
Error Comparator					
Output Leakage Current (V_{OH} = 30 V)	I_{lkg}	−	0.01	1.0	μA
Output Low Voltage (V_{in} = 4.5 V, I_{OL} = 400 μA)	V_{OL}	−	150	250	mV
Upper Threshold Voltage (V_{in} = 6.0 V)	V_{thu}	40	45	−	mV
Lower Threshold Voltage (V_{in} = 6.0 V)	V_{thl}	−	60	95	mV
Hysteresis (V_{in} = 6.0 V)	V_{hy}	−	15	−	mV
Shutdown Input					
Input Logic Voltage	V_{shtdn}				V
Logic “0” (Regulator “On”)		0	−	0.7	
Logic “1” (Regulator “Off”)		2.0	−	30	
Shutdown Pin Input Current	I_{shtdn}				μA
V_{shtdn} = 2.4 V		−	35	50	
V_{shtdn} = 30 V		−	450	600	
Regulator Output Current in Shutdown Mode (V_{in} = 30 V, V_{shtdn} = 2.0 V, V_O = 0, Pin 6 Connected to Pin 7)	I_{off}	−	3.0	10	μA

6. The Junction−to−Ambient Thermal Resistance is determined by PCB copper area per Figure 29.
7. ESD data available upon request.
8. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
9. $V_{O(nom)}$ is the part number voltage option.
10. Noise tests on the LP2951 are made with a 0.01 μF capacitor connected across Pins 7 and 1.

*NCV prefix is for automotive and other applications requiring site and change control.

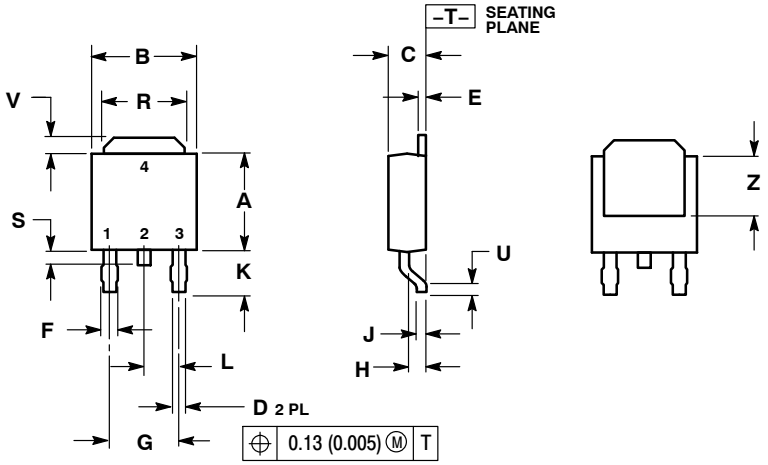
ORDERING INFORMATION (LP2950)

Part Number	Output Voltage (Volts)	Tolerance (%)	Package	Shipping†
LP2950CDT−3.3G	3.3	1.0	DPAK (Pb−Free)	75 Units / Rail
LP2950CDT−3.3RK	3.3	1.0	DPAK	2500 Units / Tape & Reel
LP2950CDT−3.3RKG	3.3	1.0	DPAK (Pb−Free)	2500 Units / Tape & Reel
LP2950ACDT−3.3	3.3	0.5	DPAK	75 Units / Rail
LP2950ACDT−3.3RG	3.3	0.5	DPAK (Pb−Free)	2500 Units / Tape & Reel
LP2950ACDT−3.3RK	3.3	0.5	DPAK	2500 Units / Tape & Reel
LP2950CDT−5.0	5.0	1.0	DPAK	75 Units / Rail
LP2950CDT−5.0G	5.0	1.0	DPAK (Pb−Free)	75 Units / Rail
LP2950CDT−5.0RK	5.0	1.0	DPAK	2500 Units / Tape & Reel
LP2950CDT−5.0RKG	5.0	1.0	DPAK (Pb−Free)	2500 Units / Tape & Reel
LP2950ACDT−5.0	5.0	0.5	DPAK	75 Units / Rail
LP2950ACDT−5.0G	5.0	0.5	DPAK (Pb−Free)	75 Units / Rail
LP2950ACDT−5.0RK	5.0	0.5	DPAK	2500 Units / Tape & Reel
LP2950ACDT−5RKG	5.0	0.5	DPAK (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

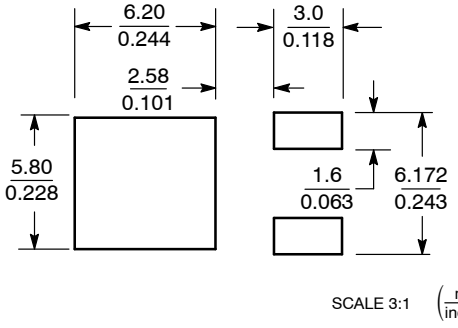
DPAK
DT SUFFIX
PLASTIC PACKAGE
CASE 369C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details please download the ON Semiconductor Soldering and Mozunting Techniques Reference Manual, SOLDERRM/D.