TL431, A, B Series, NCV431A, B

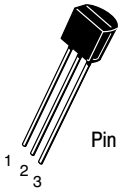
Programmable Precision References

The TL431, A, B integrated circuits are three−terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431, A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

Features

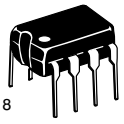
- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance: ±0.4%, Typ @ 25°C (TL431B)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full−Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- Pb−Free Packages are Available

ON Semiconductor®



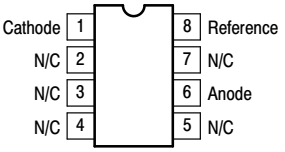
TO−92 (TO−226)
LP SUFFIX
CASE 29

Pin 1. Reference
2. Anode
3. Cathode



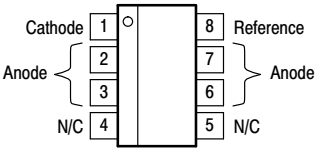
PDIP−8
P SUFFIX
CASE 626

Micro8™
DM SUFFIX
CASE 846A



(Top View)

SOIC−8
D SUFFIX
CASE 751



(Top View)

This is an internally modified SOIC−8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification increases power dissipation capability when appropriately mounted on a printed circuit board. This modified package conforms to all external dimensions of the standard SOIC−8 package.

ORDERING INFORMATION

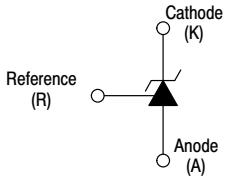
See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

DEVICE MARKING INFORMATION

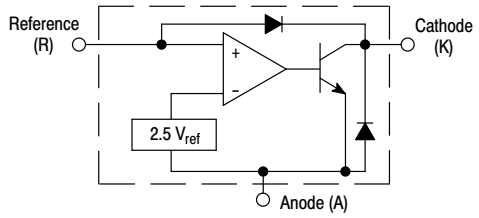
See general marking information in the device marking section on page 16 of this data sheet.

Publication Order Number:
TL431/D

Symbol

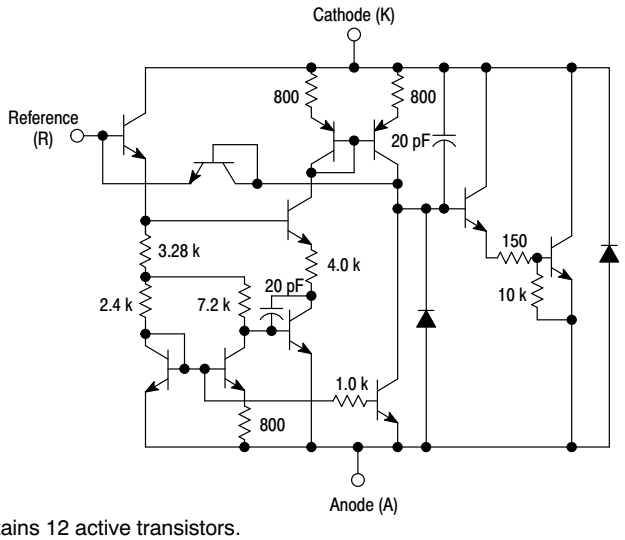


Representative Block Diagram



Representative Schematic Diagram

Component values are nominal



This device contains 12 active transistors.

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	−100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	−0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431I, TL431AI, TL431BI TL431C, TL431AC, TL431BC NCV431AI, NCV431B, TL431BV	T_A	 −40 to +85 0 to +70 −40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package DM Suffix Plastic Package	P_D	 0.70 1.10 0.52	W
Total Power Dissipation @ T_C = 25°C Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package	P_D	 1.5 3.0	W
ESD Rating	HBM MM	>2000 >200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

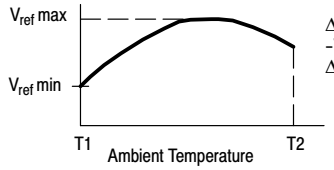
THERMAL CHARACTERISTICS

Characteristic	Symbol	D, LP Suffix Package	P Suffix Package	DM Suffix Package	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	178	114	240	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83	41	–	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431AI / NCV431AI			TL431AC			TL431BI / TL431BV NCV431BV			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) V_{KA} = V_{ref}, I_K = 10 mA T_A = 25°C T_A = T_{low} to T_{high}	V_{ref}	 2.47 2.44	 2.495 –	 2.52 2.55	 2.47 2.453	 2.495 –	 2.52 2.537	 2.483 2.475	 2.495 2.495	 2.507 2.515	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 4, 5) V_{KA}= V_{ref}, I_K = 10 mA	ΔV_{ref}	–	7.0	30	–	3.0	17	–	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	 – –	 –1.4 –1.0	 –2.7 –2.0	 – –	 –1.4 –1.0	 –2.7 –2.0	 – –	 –1.4 –1.0	 –2.7 –2.0	mV/V
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞ T_A = 25°C T_A = T_{low} to T_{high} (Note 4)	I_{ref}	 – –	 1.8 –	 4.0 6.5	 – –	 1.8 –	 4.0 5.2	 – –	 1.1 –	 2.0 4.0	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 4) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	–	0.8	2.5	–	0.4	1.2	–	0.8	2.5	μA
Minimum Cathode Current For Regulation V_{KA} = V_{ref} (Figure 1)	I_{min}	–	0.5	1.0	–	0.5	1.0	–	0.5	1.0	mA
Off–State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	–	20	1000	–	20	1000	–	0.23	500	nA
Dynamic Impedance (Figure 1, Note 6) V_{KA} = V_{ref}, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{KA}\rvert$	–	0.22	0.5	–	0.22	0.5	–	0.14	0.3	Ω

4. T_{low} = −40°C for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431BV, TL431AIDM, TL431IDM, TL431BIDM, NCV431AIDMR2, NCV431AIDR2
   = 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
   T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
   = +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
   = +125°C TL431BV, NCV431AIDMR2, NCV431AIDR2, NCV431BVDMR2G
5. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



$\Delta V_{ref} = V_{ref}$ max $- V_{ref}$ min
$\Delta T_A = T_2 - T_1$

The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref}\ \frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref}\ @\ 25°C}\right) X\ 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A\ (V_{ref} @ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C $\qquad \alpha V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8$ ppm/°C

6. The dynamic impedance Z_{KA} is defined as $\lvert Z_{KA}\rvert = \frac{\Delta V_{KA}}{\Delta I_K}$ When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as: $\lvert Z_{KA}'\rvert \approx \lvert Z_{KA}\rvert \left(1 + \frac{R1}{R2}\right)$
7. NCV431AIDMR2, NCV431AIDR2, NCV431BVDMR2G T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

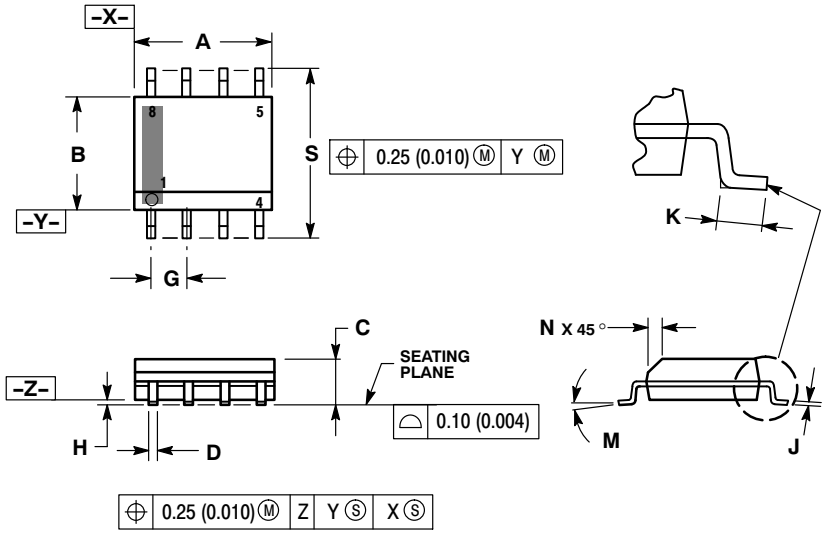
ORDERING INFORMATION

Device	Operating Temperature Range	Package Code	Shipping Information†	Tolerance
TL431ACD	0°C to 70°C	SOIC−8	98 Units / Rail	1.0%
TL431ACDG		SOIC−8 (Pb−Free)		
TL431BCD		SOIC−8		0.4%
TL431BCDG		SOIC−8 (Pb−Free)		
TL431CD		SOIC−8		2.2%
TL431CDG		SOIC−8 (Pb−Free)		
TL431ACDR2		SOIC−8	2500 Units / Tape & Reel	1.0%
TL431ACDR2G		SOIC−8 (Pb−Free)		
TL431BCDR2		SOIC−8		0.4%
TL431BCDR2G		SOIC−8 (Pb−Free)		
TL431CDR2		SOIC−8		2.2%
TL431CDR2G		SOIC−8 (Pb−Free)		
TL431ACDMR2		Micro8	4000 Units / Tape & Reel	1.0%
TL431ACDMR2G		Micro8 (Pb−Free)		1.0%
TL431BCDMR2		Micro8		0.4%
TL431BCDMR2G		Micro8 (Pb−Free)		
TL431CDMR2		Micro8		2.2%
TL431CDMR2G		Micro8 (Pb−Free)		
TL431ACP		PDIP−8	50 Units / Rail	1.0%
TL431ACPG		PDIP−8 (Pb−Free)		1.0%
TL431BCP		PDIP−8		0.4%
TL431BCPG		PDIP−8 (Pb−Free)		0.4%
TL431CP		PDIP−8		2.2%
TL431CPG		PDIP−8 (Pb−Free)		
TL431ACLP		TO−92 (TO−226)	2000 Units / Bag	1.0%
TL431ACLPG		TO−92 (TO−226) (Pb−Free)		
TL431BCLP		TO−92 (TO−226)		0.4%
TL431BCLPG		TO−92 (TO−226) (Pb−Free)		
TL431CLP		TO−92 (TO−226)		2.2%
TL431CLPG		TO−92 (TO−226) (Pb−Free)		
TL431ACLPRA		TO−92 (TO−226)	2000 Units / Tape & Reel	1.0%
TL431ACLPRAG		TO−92 (TO−226) (Pb−Free)		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

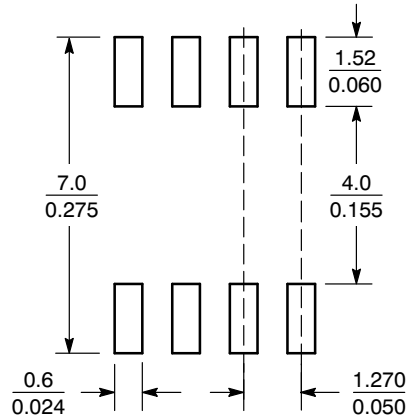
SOIC−8
D SUFFIX
PLASTIC PACKAGE
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.