MC14553B

3-Digit BCD Counter

The MC14553B 3−digit BCD counter consists of 3 negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on−chip oscillator provides the low−frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

Features

- TTL Compatible Outputs
- On−Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input Current (DC or Transient) per Pin	I_{in}	±10	mA
Output Current (DC or Transient) per Pin	I_{out}	+20	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (8−Second Soldering)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic “P and D/DW”
   Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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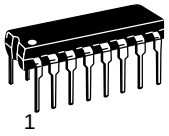
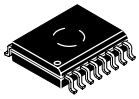
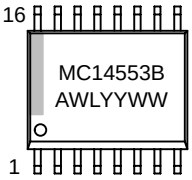
MARKING DIAGRAMS



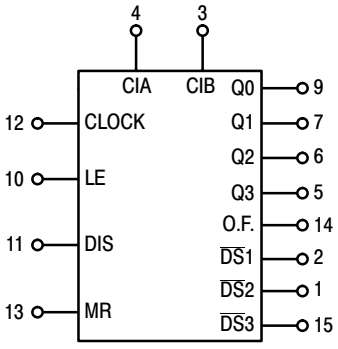
PDIP−16
P SUFFIX
CASE 648



SO−16W
DW SUFFIX
CASE 751G



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package



V_{DD} = PIN 16
V_{SS} = PIN 8

Figure 1. Block Diagram

ORDERING INFORMATION

Device	Package	Shipping
MC14553BCP	PDIP−16	25 Units / Rail
MC14553BCPG	PDIP−16 (Pb−Free)	25 Units / Rail
MC14553BDW	SOIC−16	47 Units / Rail

Publication Order Number:
MC14553B/D

TRUTH TABLE

Inputs				
Master Reset	**Clock**	**Disable**	**LE**	**Outputs**
0	↑	0	0	No Change
0	↓	0	0	Advance
0	X	1	X	No Change
0	1	↑	0	Advance
0	1	↓	0	No Change
0	0	X	X	No Change
0	X	X	↑	Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don't Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc) Source − Pin 3	I_{OH}	5.0 10 15	– 0.25 – 0.62 – 1.8	− − −	– 0.2 – 0.5 – 1.5	– 0.36 – 0.9 – 3.5	− − −	−0.14 −0.35 −1.1	− − −	mAdc
(V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc) Source − Other Outputs		5.0 10 15	– 0.64 – 1.6 – 4.2	− − −	– 0.51 – 1.3 – 3.4	– 0.88 – 2.25 – 8.8	− − −	– 0.36 – 0.9 – 2.4	− − −	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc) Sink − Pin 3	I_{OL}	5.0 10 15	0.5 1.1 1.8	− − −	0.4 0.9 1.5	0.88 2.25 8.8	− − −	0.28 0.65 1.20	− − −	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc) Sink − Other Outputs		5.0 10 15	3.0 6.0 18	− − −	2.5 5.0 15	4.0 8.0 20	− − −	1.6 3.5 10	− − −	mAdc
Input Current	I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package) MR = V_{DD}	I_{DD}	5.0 10 15	− − −	5.0 10 20	− − −	0.010 0.020 0.030	5.0 10 20	− − −	150 300 600	μAdc
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.35 μA/kHz) f + I_{DD} I_T = (0.85 μA/kHz) f + I_{DD} I_T = (1.50 μA/kHz) f + I_{DD}							μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L - 50)$ Vfk where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

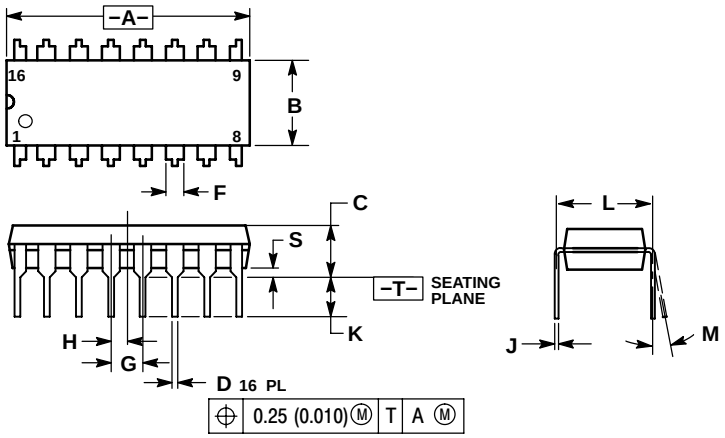
SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	2a	t_{TLH}, t_{THL}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Clock to BCD Out	2a	t_{PLH}, t_{PHL}	5.0 10 15	– – –	900 500 200	1800 1000 400	ns
Clock to Overflow	2a	t_{PHL}	5.0 10 15	– – –	600 400 200	1200 800 400	ns
Reset to BCD Out	2b	t_{PHL}	5.0 10 15	– – –	900 500 300	1800 1000 600	ns
Clock to Latch Enable Setup Time Master Reset to Latch Enable Setup Time	2b	t_{su}	5.0 10 15	600 400 200	300 200 100	– – –	ns
Removal Time Latch Enable to Clock	2b	t_{rem}	5.0 10 15	– 80 – 10 0	– 200 – 70 – 50	– – –	ns
Clock Pulse Width	2a	$t_{WH(cl)}$	5.0 10 15	550 200 150	275 100 75	– – –	ns
Reset Pulse Width	2b	$t_{WH(R)}$	5.0 10 15	1200 600 450	600 300 225	– – –	ns
Reset Removal Time	–	t_{rem}	5.0 10 15	– 80 0 20	– 180 – 50 – 30	– – –	ns
Input Clock Frequency	2a	f_{cl}	5.0 10 15	– – –	1.5 5.0 7.0	0.9 2.5 3.5	MHz
Input Clock Rise Time	2b	t_{TLH}	5.0 10 15	No Limit			ns
Disable, MR, Latch Enable Rise and Fall Times	–	t_{TLH}, t_{THL}	5.0 10 15	– – –	– – –	15 5.0 4.0	μs
Scan Oscillator Frequency (C1 measured in μF)	1	f_{osc}	5.0 10 15	– – –	1.5/C1 4.2/C1 7.0/C1	– – –	Hz

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

PACKAGE DIMENSIONS

PDIP−16
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01