MC14490

Hex Contact Bounce Eliminator

The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R−C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490 (see Figure 5).

NOTE: Immediately after powerup, the outputs of the MC14490 are in indeterminate states.

Features

- Diode Protection on All Inputs
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay Line
- Internal Oscillator (R−C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V
- Chip Complexity: 546 FETs or 136.5 Equivalent Gates
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input Current (DC or Transient) per Pin	I_{in}	±10	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (8−Second Soldering)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

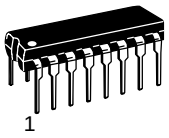
1. Temperature Derating: Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

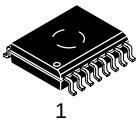
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ON Semiconductor®

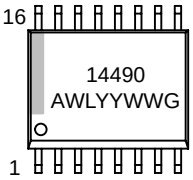
MARKING DIAGRAMS

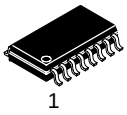


PDIP−16
P SUFFIX
CASE 648

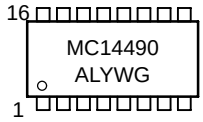


SOIC−16
DW SUFFIX
CASE 751G





SOEIAJ−16
F SUFFIX
CASE 966



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Publication Order Number:
MC14490/D

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) “1 Level” (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current Oscillator Output Source (V_{OH} = 2.5 V) (V_{OH} = 4.6 V) (V_{OH} = 9.5 V) (V_{OH} = 13.5 V)	I_{OH}	5.0 5.0 10 15	− 0.6 − 0.12 − 0.23 − 1.4	− − − −	− 0.5 − 0.1 − 0.2 − 1.2	− 1.5 − 0.3 − 0.8 − 3.0	− − − −	− 0.4 − 0.08 − 0.16 − 1.0	− − − −	mAdc
Debounce Outputs (V_{OH} = 2.5 V) (V_{OH} = 4.6 V) (V_{OH} = 9.5 V) (V_{OH} = 13.5 V)		5.0 5.0 10 15	− 0.9 − 0.19 − 0.6 1.8	− − − −	− 0.75 − 0.16 − 0.5 − 1.5	− 2.2 − 0.46 − 1.2 − 4.5	− − − −	− 0.6 − 0.12 − 0.4 − 1.2	− − − −	
Oscillator Output Sink (V_{OL} = 0.4 V) (V_{OL} = 0.5 V) (V_{OL} = 1.5 V)	I_{OL}	5.0 10 15	0.36 0.9 4.2	− − −	0.3 0.75 3.5	0.9 2.3 10	− − −	0.24 0.6 2.8	− − −	mAdc
Debounce Outputs (V_{OL} = 0.4 V) (V_{OL} = 0.5 V) (V_{OL} = 1.5 V)		5.0 10 15	2.6 4.0 12	− − −	2.2 3.3 10	4.0 9.0 35	− − −	1.8 2.7 8.1	− − −	
Input Current Debounce Inputs (V_{in} = V_{DD})	I_{IH}	15	−	2.0	−	0.2	2.0	−	11	μAdc
Input Current Oscillator — Pin 7 (V_{in} = V_{SS} or V_{DD})	I_{in}	15	−	± 620	−	± 255	± 400	−	± 250	μAdc
Pullup Resistor Source Current Debounce Inputs (V_{in} = V_{SS})	I_{IL}	5.0 10 15	175 340 505	375 740 1100	140 280 415	190 380 570	255 500 750	70 145 215	225 440 660	μAdc
Input Capacitance	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (V_{in} = V_{SS} or V_{DD}, I_{out} = 0 μA)	I_{SS}	5.0 10 15	− − −	150 280 840	− − −	40 90 225	100 225 650	− − −	90 180 550	μAdc

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

SWITCHING CHARACTERISTICS (Note 3) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 4)	Max	Unit
Output Rise Time All Outputs	t_{TLH}	5.0 10 15	– – –	180 90 65	360 180 130	ns
Output Fall Time — Oscillator Output	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Debounce Outputs	t_{THL}	5.0 10 15	– – –	60 30 20	120 60 40	
Propagation Delay Time Oscillator Input to Debounce Outputs	t_{PHL}	5.0 10 15	– – –	285 120 95	570 240 190	ns
	t_{PLH}	5.0 10 15	– – –	370 160 120	740 320 240	
Clock Frequency (50% Duly Cycle) (External Clock)	f_{cl}	5.0 10 15	– – –	2.8 6 9	1.4 3.0 4.5	MHz
Setup Time (See Figure 1)	t_{su}	5.0 10 15	100 80 60	50 40 30	– – –	ns
Maximum External Clock Input Rise and Fall Time Oscillator Input	t_r, t_f	5.0 10 15	No Limit			ns
Oscillator Frequency OSC_{out} $C_{ext} \geq$ 100 pF* Note: These equations are intended to be a design guide. Laboratory experimentation may be required. Formulas are typically ± 15% of actual frequencies.	f_{osc}, typ	5.0 10 15	$\frac{1.5}{C_{ext}\ (\text{in}\ \mu F)}$ $\frac{4.5}{C_{ext}\ (\text{in}\ \mu F)}$ $\frac{6.5}{C_{ext}\ (\text{in}\ \mu F)}$			Hz

3. The formulas given are for the typical characteristics only at 25°C.
4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

***POWER−DOWN CONSIDERATIONS**

Large values of C_{ext} may cause problems when powering down the MC14490 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge through the input protection diodes at Pin 7 or the parasitic diodes at Pin 9. Current through these internal diodes must be limited to 10 mA, therefore the turn−off time of the power supply must not be faster than $t = (V_{DD} - V_{SS}) \bullet C_{ext}/(10\ mA)$. For example, If $V_{DD} - V_{SS}$ = 15 V and C_{ext} = 1 μF, the power supply must turn off no faster than t = (15 V) • (1 μF)/10 mA = 1.5 ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of the power supply to zero volts occurs, the MC14490 may sustain damage. To avoid this possibility, use external clamping diodes, D1 and D2, connected as shown in Figure 2.

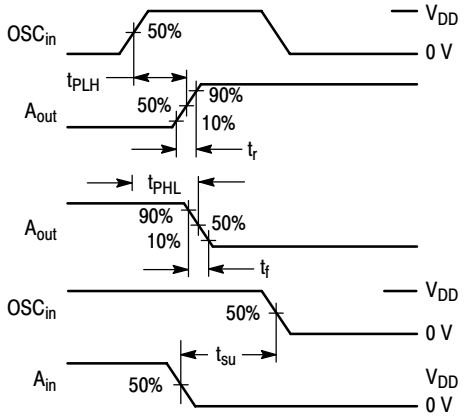


Figure 1. Switching Waveforms

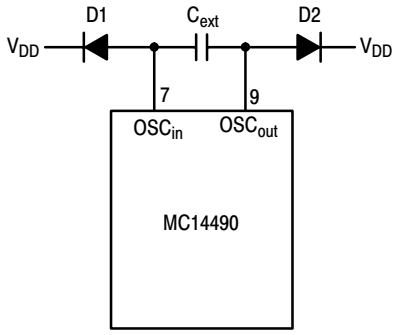


Figure 2. Discharge Protection During Power Down

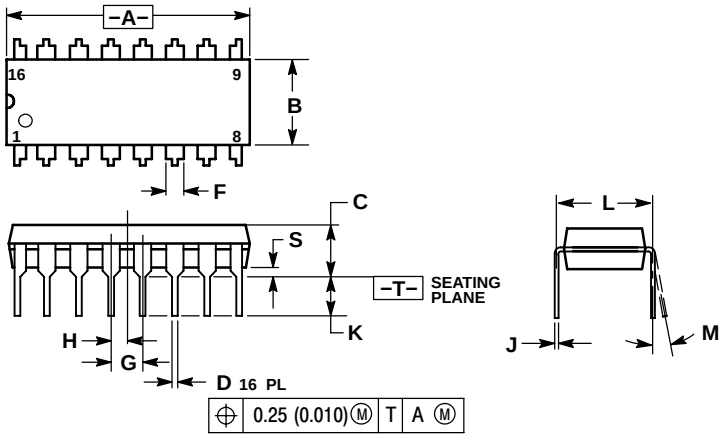
ORDERING INFORMATION

Device	Package	Shipping†
MC14490DW	SOIC−16	47 Units / Rail
MC14490DWG	SOIC−16 (Pb−Free)	
MC14490DWR2	SOIC−16	1000 / Tape & Reel
MC14490DWR2G	SOIC−16 (Pb−Free)	
MC14490F	SOEIAJ−16	50 Units / Rail
MC14490FG	SOEIAJ−16 (Pb−Free)	
MC14490FEL	SOEIAJ−16	2000 Units / Tape & Reel
MC14490FELG	SOEIAJ−16 (Pb−Free)	
MC14490P	PDIP−16	25 Units / Rail
MC14490PG	PDIP−16 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

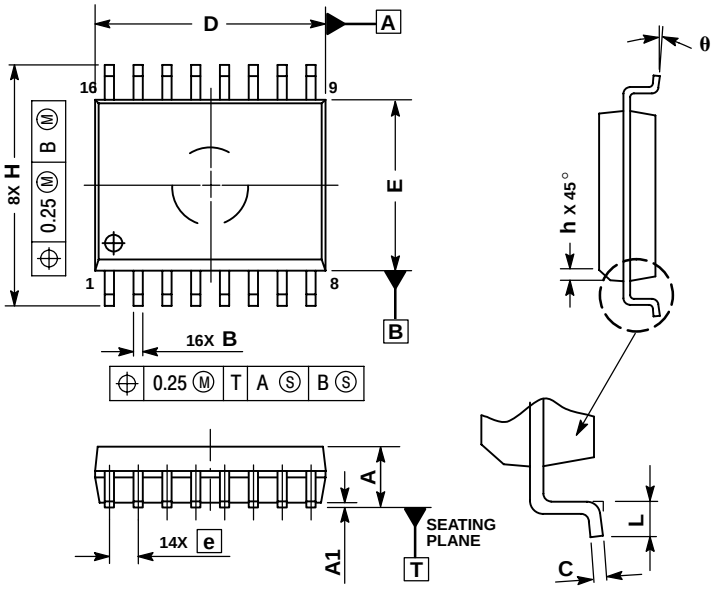
PDIP−16
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SO−16 WB
CASE 751G−03
ISSUE C



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0 °	7 °