# MC14093B

# Quad 2-Input "NAND" Schmitt Trigger

The MC14093B Schmitt trigger is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2−input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

**ON Semiconductor®**

## Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin−for−Pin Compatible with CD4093
- Can be Used to Replace MC14011B
- Independent Schmitt−Trigger at each Input
- Pb−Free Packages are Available

## MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8−Second Soldering) | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Temperature Derating:
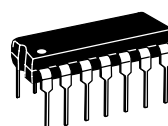   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.
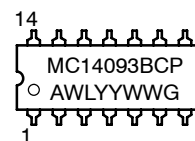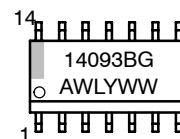
## MARKING DIAGRAMS



**PDIP−14**
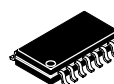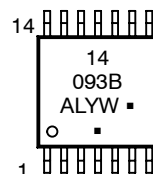**P SUFFIX**
**CASE 646**

```
14
MC14093BCP
○ AWLYYWWG
1
```

**SOIC−14**
**D SUFFIX**
**CASE 751A**

```
14
14093BG
○ AWLYWW
1
```

**TSSOP−14**
**DT SUFFIX**
**CASE 948G**

```
14
14
093B
ALYW ▪
○
1
```

**SOEIAJ−14**
**F SUFFIX**
**CASE 965**

```
14
MC14093B
○ ALYWG
1
```
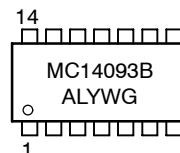
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC14093B

## PIN ASSIGNMENT

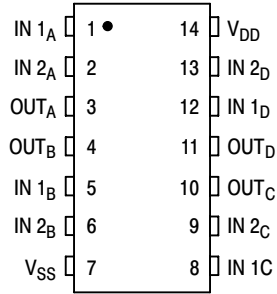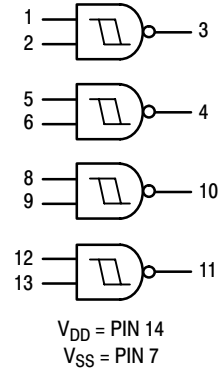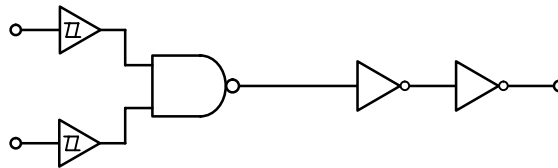| | | | |
|---|---|---|---|
| IN 1$_A$ | 1 • | 14 | V$_{DD}$ |
| IN 2$_A$ | 2 | 13 | IN 2$_D$ |
| OUT$_A$ | 3 | 12 | IN 1$_D$ |
| OUT$_B$ | 4 | 11 | OUT$_D$ |
| IN 1$_B$ | 5 | 10 | OUT$_C$ |
| IN 2$_B$ | 6 | 9 | IN 2$_C$ |
| V$_{SS}$ | 7 | 8 | IN 1C |

## LOGIC DIAGRAM

1
2 → 3

5
6 → 4

8
9 → 10

12
13 → 11

V$_{DD}$ = PIN 14
V$_{SS}$ = PIN 7

## EQUIVALENT CIRCUIT SCHEMATIC
### (1/4 OF CIRCUIT SHOWN)

## ORDERING INFORMATION

| Device | Package | Shipping[†] |
|---|---|---|
| MC14093BCP | PDIP−14 | 25 Units / Rail |
| MC14093BCPG | PDIP−14 (Pb−Free) | |
| MC14093BD | SOIC−14 | 55 Units / Rail |
| MC14093BDG | SOIC−14 (Pb−Free) | |
| MC14093BDR2 | SOIC−14 | 2500 Units / Tape & Reel |
| MC14093BDR2G | SOIC−14 (Pb−Free) | |
| MC14093BDTR2 | TSSOP−14* | |
| MC14093BDTR2G | TSSOP−14* | |
| MC14093BFEL | SOEIAJ−14 | 2000 Units / Tape & Reel |
| MC14093BFELG | SOEIAJ−14 (Pb−Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

# MC14093B

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | – 55°C Min | – 55°C Max | 25°C Min | 25°C Typ [2] | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage "0" Level $V_{in} = V_{DD}$ or 0 | $V_{OL}$ | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| "1" Level $V_{in} = 0$ or $V_{DD}$ | $V_{OH}$ | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | |
| | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | |
| Output Drive Current ($V_{OH}$ = 2.5 Vdc) Source | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) | | 5.0 | – 3.0 | – | – 2.4 | – 4.2 | – | – 1.7 | – | |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | – 0.64 | – | – 0.51 | – 0.88 | – | – 0.36 | – | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | – 1.6 | – | – 1.3 | – 2.25 | – | – 0.9 | – | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | – 4.2 | – | – 3.4 | – 8.8 | – | – 2.4 | – | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | |
| Input Current | $I_{in}$ | 15 | – | ± 0.1 | – | ± 0.00001 | ± 0.1 | – | ± 1.0 | μAdc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | – | 0.25 | – | 0.0005 | 0.25 | – | 7.5 | μAdc |
| | | 10 | – | 0.5 | – | 0.0010 | 0.5 | – | 15 | |
| | | 15 | – | 1.0 | – | 0.0015 | 1.0 | – | 30 | |
| Total Supply Current [3] [4] (Dynamic plus Quiescent, Per Package) ($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0 | | | $I_T = $ (1.2 μA/kHz) f + $I_{DD}$ | | | | | μAdc |
| | | 10 | | | $I_T = $ (2.4 μA/kHz) f + $I_{DD}$ | | | | | |
| | | 15 | | | $I_T = $ (3.6 μA/kHz) f + $I_{DD}$ | | | | | |
| Hysteresis Voltage | $V_H$† | 5.0 | 0.3 | 2.0 | 0.3 | 1.1 | 2.0 | 0.3 | 2.0 | Vdc |
| | | 10 | 1.2 | 3.4 | 1.2 | 1.7 | 3.4 | 1.2 | 3.4 | |
| | | 15 | 1.6 | 5.0 | 1.6 | 2.1 | 5.0 | 1.6 | 5.0 | |
| Threshold Voltage Positive–Going | $V_{T+}$ | 5.0 | 2.2 | 3.6 | 2.2 | 2.9 | 3.6 | 2.2 | 3.6 | Vdc |
| | | 10 | 4.6 | 7.1 | 4.6 | 5.9 | 7.1 | 4.6 | 7.1 | |
| | | 15 | 6.8 | 10.8 | 6.8 | 8.8 | 10.8 | 6.8 | 10.8 | |
| Negative–Going | $V_{T–}$ | 5.0 | 0.9 | 2.8 | 0.9 | 1.9 | 2.8 | 0.9 | 2.8 | Vdc |
| | | 10 | 2.5 | 5.2 | 2.5 | 3.9 | 5.2 | 2.5 | 5.2 | |
| | | 15 | 4.0 | 7.4 | 4.0 | 5.8 | 7.4 | 4.0 | 7.4 | |

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L – 50) \text{ Vfk}$$

where: $I_T$ is in μA (per package), $C_L$ in pF, V = ($V_{DD} – V_{SS}$) in volts, f in kHz is input frequency, and k = 0.004.

**SWITCHING CHARACTERISTICS** ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ [5] | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | 5.0 | – | 100 | 200 | ns |
| | | 10 | – | 50 | 100 | |
| | | 15 | – | 40 | 80 | |
| Output Fall Time | $t_{THL}$ | 5.0 | – | 100 | 200 | ns |
| | | 10 | – | 50 | 100 | |
| | | 15 | – | 40 | 80 | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | 5.0 | – | 125 | 250 | ns |
| | | 10 | – | 50 | 100 | |
| | | 15 | – | 40 | 80 | |

5.  Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
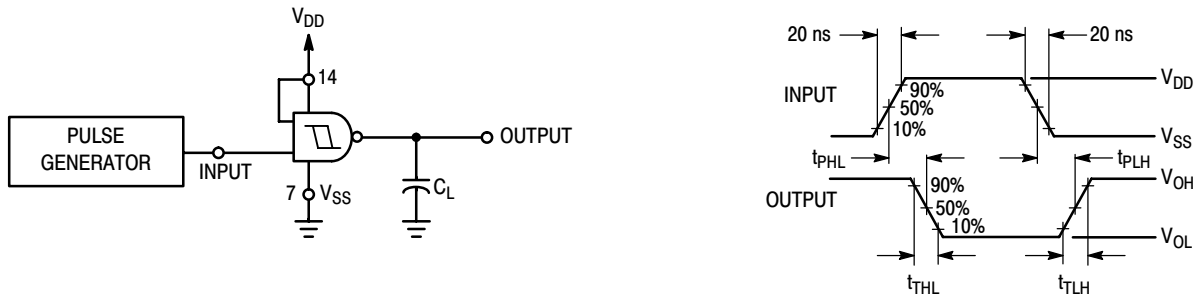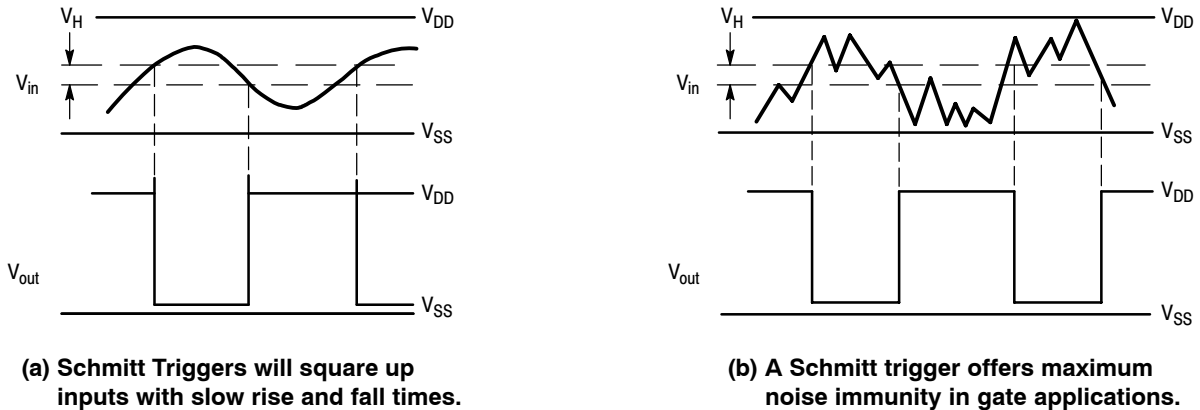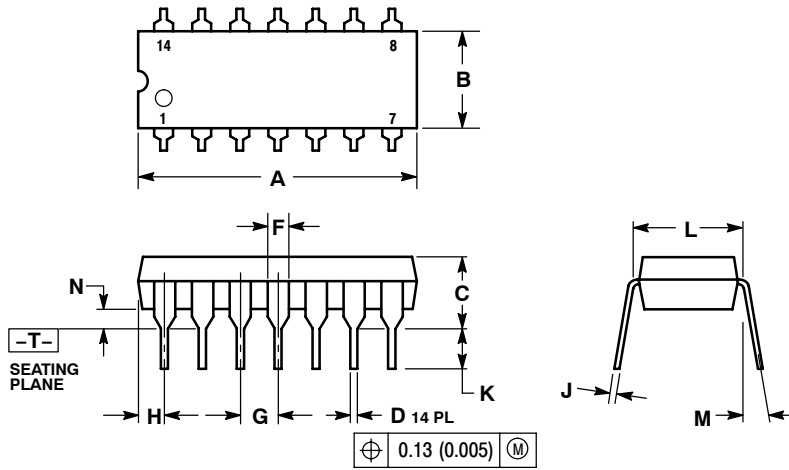


**Figure 1. Switching Time Test Circuit and Waveforms**



(a) Schmitt Triggers will square up
   inputs with slow rise and fall times.

(b) A Schmitt trigger offers maximum
   noise immunity in gate applications.

**Figure 2. Typical Schmitt Trigger Applications**

# MC14093B

## PACKAGE DIMENSIONS

**PDIP−14**
CASE 646−06
ISSUE P

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|--------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | ――― | 10 ° | ――― | 10 ° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |