MC14049B, MC14050B

Hex Buffer

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage, V_{DD}.

The input–signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS–to–TTL/DTL converter ($V_{DD} = 5.0$ V, $V_{OL} \leq 0.4$ V, $I_{OL} \geq 3.2$ mA).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

Features

- High Source and Sink Currents
- High–to–Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- V_{IN} can exceed V_{DD}
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs
- Pb–Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Pin	±10	mA
I_{out}	Output Current (DC or Transient) per Pin	±45	mA
P_D	Power Dissipation, per Package (Note 1) (Plastic) (SOIC)	825 740	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

1. Temperature Derating: See Figure 3.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high–impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18$ V and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
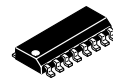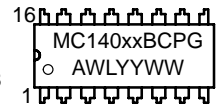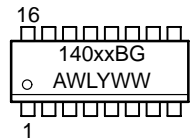
ON Semiconductor®

MARKING DIAGRAMS

PDIP–16
P SUFFIX
CASE 648

16
MC140xxBCPG
○ AWLYYWW
1
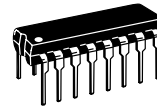
SOIC–16
D SUFFIX
CASE 751B

16
140xxBG
○ AWLYWW
1

TSSOP–16
DT SUFFIX
CASE 948F

16
14
0xxB
○ ALYW
1
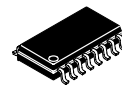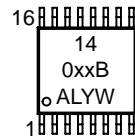
SOEIAJ–16
F SUFFIX
CASE 966

16
MC140xxB
○ ALYWG
1
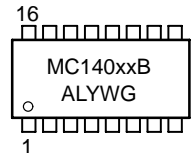
xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb–Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14049B, MC14050B

PIN ASSIGNMENT

V_DD	1 ●	16	NC
OUT_A	2	15	OUT_F
IN_A	3	14	IN_F
OUT_B	4	13	NC
IN_B	5	12	OUT_E
OUT_C	6	11	IN_E
IN_C	7	10	OUT_D
V_SS	8	9	IN_D

LOGIC DIAGRAM

MC14049B

3 → 2
5 → 4
7 → 6
9 → 10
11 → 12
14 → 15

NC = PIN 13, 16
V_{SS} = PIN 8
V_{DD} = PIN 1

MC14050B

3 → 2
5 → 4
7 → 6
9 → 10
11 → 12
14 → 15

NC = PIN 13, 16
V_{SS} = PIN 8
V_{DD} = PIN 1
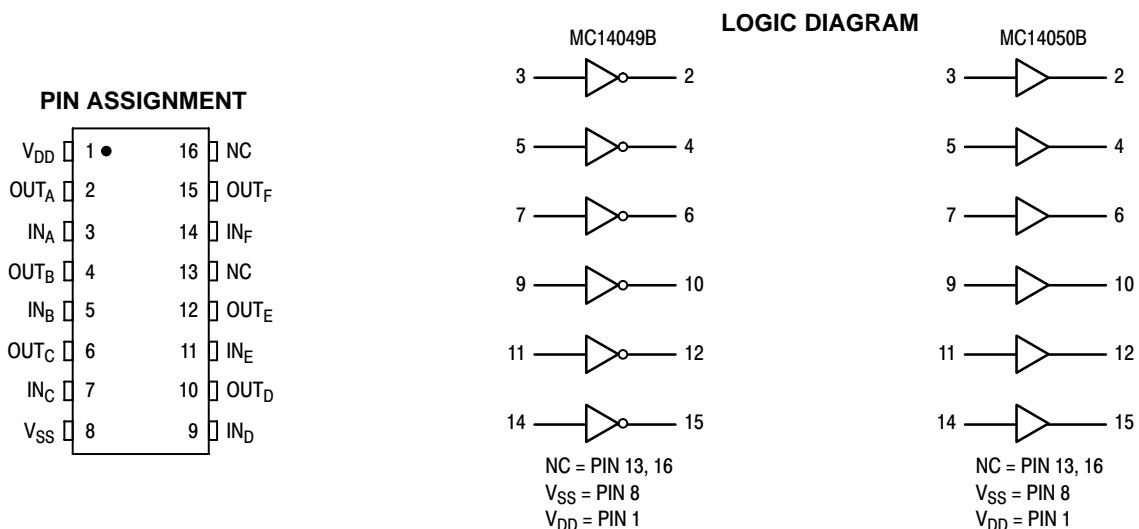
ORDERING INFORMATION

Device	Package	Shipping†
MC14049BCP	PDIP–16	500 Units / Rail
MC14049BCPG	PDIP–16 (Pb–Free)	500 Units / Rail
MC14049BD	SOIC–16	48 Units / Rail
MC14049BDG	SOIC–16 (Pb–Free)	48 Units / Rail
MC14049BDR2	SOIC–16	2500 Units / Tape & Reel
MC14049BDR2G	SOIC–16 (Pb–Free)	2500 Units / Tape & Reel
MC14049BFEL	SOEIAJ–16	2000 Units / Tape & Reel
MC14050BCP	PDIP–16	500 Units / Rail
MC14050BCPG	PDIP–16 (Pb–Free)	500 Units / Rail
MC14050BD	SOIC–16	48 Units / Rail
MC14050BDR2	SOIC–16	2500 Units / Tape & Reel
MC14050BDR2G	SOIC–16 (Pb–Free)	2500 Units / Tape & Reel
MC14050BDT	TSSOP–16*	96 Units / Rail
MC14050BDTR2	TSSOP–16*	2500 Units / Tape & Reel
MC14050BFEL	SOEIAJ–16	2000 Units / Tape & Reel
MC14050BFELG	SOEIAJ–16 (Pb–Free)	2000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb–Free.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V$_{SS}$)

Characteristic		Symbol	V$_{DD}$ Vdc	− 55°C		+ 25°C			+ 125°C		Unit
				Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage "0" Level V$_{in}$ = V$_{DD}$	"0" Level	V$_{OL}$	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V$_{in}$ = 0	"1" Level	V$_{OH}$	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
Input Voltage "0" Level (V$_O$ = 4.5 Vdc) (V$_O$ = 9.0 Vdc) (V$_O$ = 13.5 Vdc)	"0" Level	V$_{IL}$	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
"1" Level (V$_O$ = 0.5 Vdc) (V$_O$ = 1.0 Vdc) (V$_O$ = 1.5 Vdc)	"1" Level	V$_{IH}$	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current (V$_{OH}$ = 2.5 Vdc) (V$_{OH}$ = 9.5 Vdc) (V$_{OH}$ = 13.5 Vdc)	Source	I$_{OH}$	5.0 10 15	− 1.6 − 1.6 − 4.7	– – –	− 1.25 − 1.30 − 3.75	− 2.5 − 2.6 − 10	– – –	− 1.0 − 1.0 − 3.0	– – –	mAdc
(V$_{OL}$ = 0.4 Vdc) (V$_{OL}$ = 0.5 Vdc) (V$_{OL}$ = 1.5 Vdc)	Sink	I$_{OL}$	5.0 10 15	3.75 10 30	– – –	3.2 8.0 24	6.0 16 40	– – –	2.6 6.6 19	– – –	mAdc
Input Current		I$_{in}$	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	µAdc
Input Capacitance (V$_{in}$ = 0)		C$_{in}$	–	–	–	–	10	20	–	–	pF
Quiescent Current (Per Package)		I$_{DD}$	5.0 10 15	– – –	1.0 2.0 4.0	– – –	0.002 0.004 0.006	1.0 2.0 4.0	– – –	30 60 120	µAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, per package) (C$_L$ = 50 pF on all outputs, all buffers switching		I$_T$	5.0 10 15	I$_T$ = (1.8 µA/kHz) f + I$_{DD}$ I$_T$ = (3.5 µA/kHz) f + I$_{DD}$ I$_T$ = (5.3 µA/kHz) f + I$_{DD}$							µAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at + 25°C
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

Where: I$_T$ is in µA (per Package), C$_L$ in pF, V = (V$_{DD}$ − V$_{SS}$) in volts, f in kHz is input frequency and k = 0.002.

AC SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = + 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time t_{TLH} = (0.7 ns/pF) C_L + 65 ns t_{TLH} = (0.25 ns/pF) C_L + 37.5 ns t_{TLH} = (0.2 ns/pF) C_L + 30 ns	t_{TLH}	 5.0 10 15	 – – –	 100 50 40	 160 80 60	ns
Output Fall Time t_{THL} = (0.2 ns/pF) C_L + 30 ns t_{THL} = (0.06 ns/pF) C_L + 17 ns t_{THL} = (0.04 ns/pF) C_L + 13 ns	t_{THL}	 5.0 10 15	 – – –	 40 20 15	 60 40 30	ns
Propagation Delay Time t_{PLH} = (0.33 ns/pF) C_L + 63.5 ns t_{PLH} = (0.19 ns/pF) C_L + 30.5 ns t_{PLH} = (0.06 ns/pF) C_L + 27 ns	t_{PLH}	 5.0 10 15	 – – –	 80 40 30	 140 80 60	ns
Propagation Delay Time t_{PHL} = (0.2 ns/pF) C_L + 30 ns t_{PHL} = (0.1 ns/pF) C_L + 15 ns t_{PHL} = (0.05 ns/pF) C_L + 12.5 ns	t_{PHL}	 5.0 10 15	 – – –	 40 20 15	 80 40 30	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

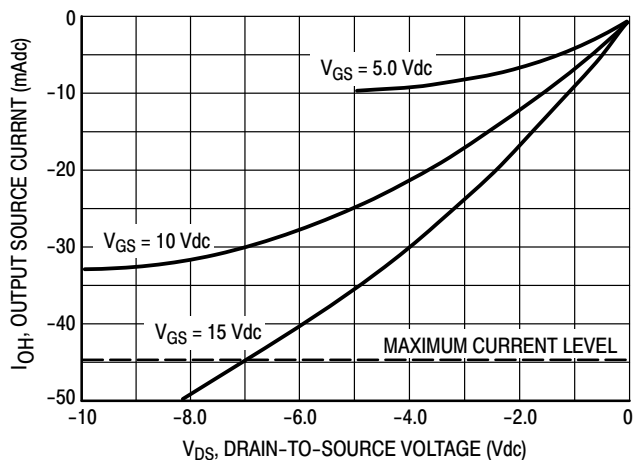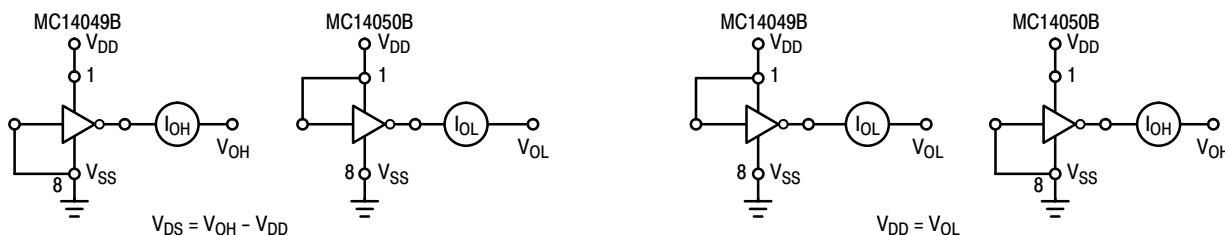
$V_{DS} = V_{OH} - V_{DD}$

$V_{DD} = V_{OL}$

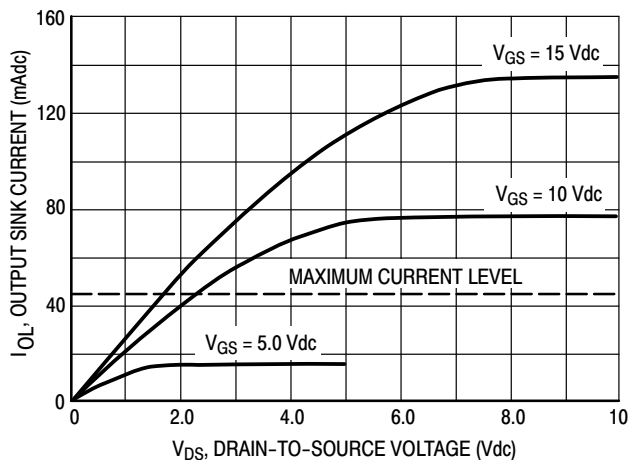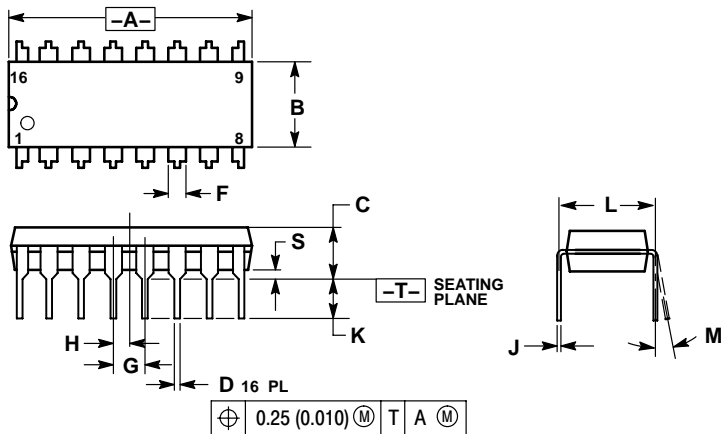Figure 1. Typical Output Source Characteristics

Figure 2. Typical Output Sink Characteristics

MC14049B, MC14050B

PACKAGE DIMENSIONS

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE T

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC–16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J
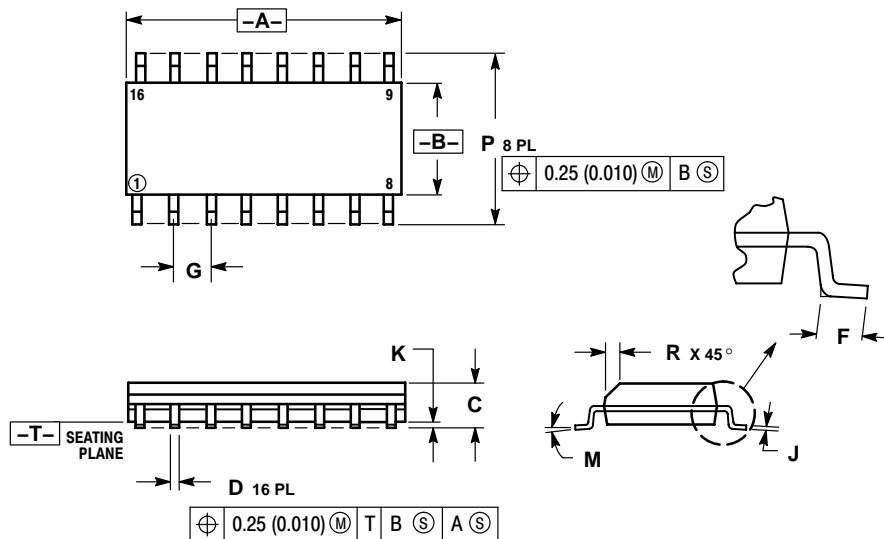
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019