



# MICROCHIP MCP6281/1R/2/3/4/5

## 450 $\mu$ A, 5 MHz Rail-to-Rail Op Amp

### Features

- Gain Bandwidth Product: 5 MHz (typical)
- Supply Current:  $I_Q = 450 \mu\text{A}$  (typical)
- Supply Voltage: 2.2V to 6.0V
- Rail-to-Rail Input/Output
- Extended Temperature Range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Available in Single, Dual, and Quad Packages
- Single with  $\overline{\text{CS}}$  (**MCP6283**)
- Dual with  $\overline{\text{CS}}$  (**MCP6285**)

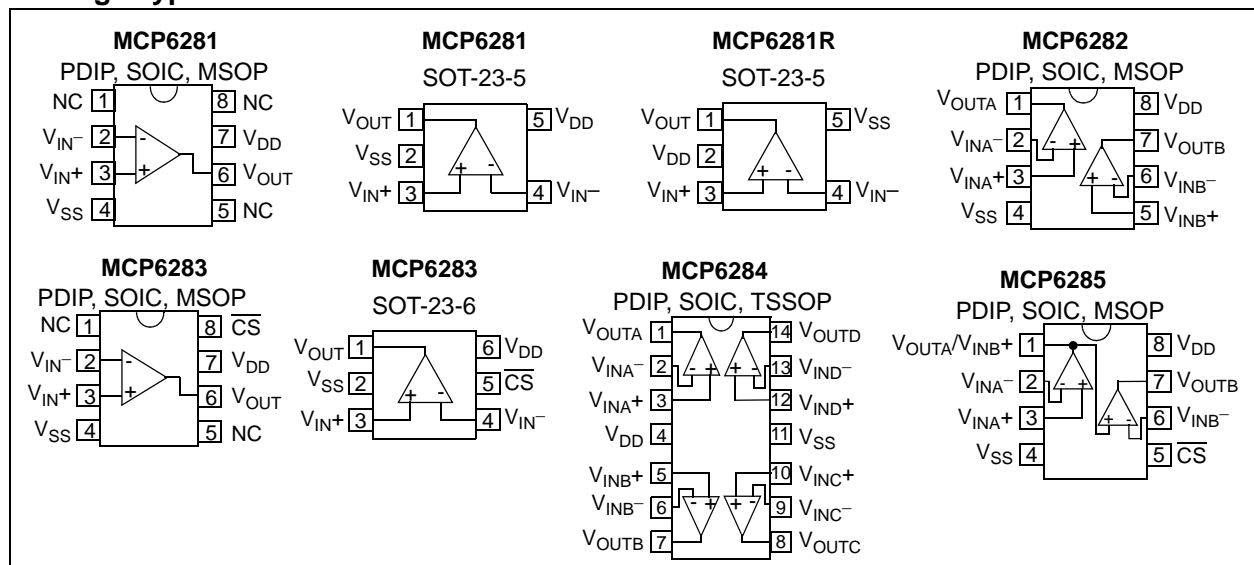
### Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

### Design Aids

- SPICE Macro Models
- FilterLab<sup>®</sup> Software
- Mindi<sup>™</sup> Circuit Designer & Simulator
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

### Package Types



### Description

The Microchip Technology Inc. MCP6281/1R/2/3/4/5 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 5 MHz Gain Bandwidth Product (GBWP) and a  $65^\circ$  phase margin. This family also operates from a single supply voltage as low as 2.2V, while drawing 450  $\mu\text{A}$  (typical) quiescent current. Additionally, the MCP6281/1R/2/3/4/5 supports rail-to-rail input and output swing, with a common mode input voltage range of  $V_{DD} + 300 \text{ mV}$  to  $V_{SS} - 300 \text{ mV}$ . This family of operational amplifiers is designed with Microchip's advanced CMOS process.

The MCP6285 has a Chip Select ( $\overline{\text{CS}}$ ) input for dual op amps in an 8-pin package. This device is manufactured by cascading the two op amps (the output of op amp A connected to the non-inverting input of op amp B). The  $\overline{\text{CS}}$  input puts the device in Low-power mode.

The MCP6281/1R/2/3/4/5 family operates over the Extended Temperature Range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . It also has a power supply range of 2.2V to 6.0V.

# MCP6281/1R/2/3/4/5

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....	7.0V
Current at Input Pins .....	$\pm 2$ mA
Analog Inputs ( $V_{IN+}$ , $V_{IN-}$ ) †† .....	$V_{SS} - 1.0V$ to $V_{DD} + 1.0V$
All Other Inputs and Outputs .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage .....	$ V_{DD} - V_{SS} $
Output Short Circuit Current .....	Continuous
Current at Output and Supply Pins .....	$\pm 30$ mA
Storage Temperature.....	$-65^{\circ}C$ to $+150^{\circ}C$
Maximum Junction Temperature ( $T_J$ ) .....	$+150^{\circ}C$
ESD Protection On All Pins (HBM; MM) .....	$\geq 4$ kV; 400V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See Section 4.1.2 “Input Voltage and Current Limits”.

### DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}C$ , $V_{DD} = +2.2V$ to $+5.5V$ , $V_{SS} = GND$ , $V_{OUT} \approx V_{DD}/2$ , $V_{CM} = V_{DD}/2$ , $V_L = V_{DD}/2$ , $R_L = 10\text{ k}\Omega$ to $V_L$ and CS is tied low. (refer to Figure 1-2 and Figure 1-3).						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Input Offset</b>						
Input Offset Voltage	$V_{OS}$	-3.0	—	+3.0	mV	$V_{CM} = V_{SS}$ (Note 1)
Input Offset Voltage (Extended Temperature)	$V_{OS}$	-5.0	—	+5.0	mV	$T_A = -40^{\circ}C$ to $+125^{\circ}C$ , $V_{CM} = V_{SS}$ (Note 1)
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	$\pm 1.7$	—	$\mu V/^{\circ}C$	$T_A = -40^{\circ}C$ to $+125^{\circ}C$ , $V_{CM} = V_{SS}$ (Note 1)
Power Supply Rejection Ratio	PSRR	70	90	—	dB	$V_{CM} = V_{SS}$ (Note 1)
<b>Input Bias, Input Offset Current and Impedance</b>						
Input Bias Current	$I_B$	—	$\pm 1.0$	—	pA	Note 2
At Temperature	$I_B$	—	50	200	pA	$T_A = +85^{\circ}C$ (Note 2)
At Temperature	$I_B$	—	2	5	nA	$T_A = +125^{\circ}C$ (Note 2)
Input Offset Current	$I_{OS}$	—	$\pm 1.0$	—	pA	Note 3
Common Mode Input Impedance	$Z_{CM}$	—	$10^{13}  6$	—	$\Omega  pF$	Note 3
Differential Input Impedance	$Z_{DIFF}$	—	$10^{13}  3$	—	$\Omega  pF$	Note 3
<b>Common Mode (Note 4)</b>						
Common Mode Input Range	$V_{CMR}$	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common Mode Rejection Ratio	CMRR	70	85	—	dB	$V_{CM} = -0.3V$ to $2.5V$ , $V_{DD} = 5V$
Common Mode Rejection Ratio	CMRR	65	80	—	dB	$V_{CM} = -0.3V$ to $5.3V$ , $V_{DD} = 5V$
<b>Open-Loop Gain</b>						
DC Open-Loop Gain (Large Signal)	$A_{OL}$	90	110	—	dB	$V_{OUT} = 0.2V$ to $V_{DD} - 0.2V$ , $V_{CM} = V_{SS}$ (Note 1)
<b>Output</b>						
Maximum Output Voltage Swing	$V_{OL}$ , $V_{OH}$	$V_{SS} + 15$	—	$V_{DD} - 15$	mV	0.5V input overdrive
Output Short Circuit Current	$I_{SC}$	—	$\pm 25$	—	mA	
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	2.2	—	6.0	V	(Note 5)
Quiescent Current per Amplifier	$I_Q$	300	450	570	$\mu A$	$I_O = 0$

- Note 1:** The MCP6285's  $V_{CM}$  for op amp B (pins  $V_{OUTA}/V_{INB+}$  and  $V_{INB-}$ ) is  $V_{SS} + 100$  mV.
- Note 2:** The current at the MCP6285's  $V_{INB-}$  pin is specified by  $I_B$  only.
- Note 3:** This specification does not apply to the MCP6285's  $V_{OUTA}/V_{INB+}$  pin.
- Note 4:** The MCP6285's  $V_{INB-}$  pin (op amp B) has a common mode range ( $V_{CMR}$ ) of  $V_{SS} + 100$  mV to  $V_{DD} - 100$  mV. The MCP6285's  $V_{OUTA}/V_{INB+}$  pin (op amp B) has a voltage range specified by  $V_{OH}$  and  $V_{OL}$ .
- Note 5:** All parts with date codes November 2007 and later have been screened to ensure operation at  $V_{DD} = 6.0V$ . However, the other minimum and maximum specifications are measured at 2.4V and/or 5.5V.

## AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.2\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_{CM} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$ ,  $C_L = 60\text{ pF}$  and  $\overline{\text{CS}}$  is tied low. (refer to [Figure 1-2](#) and [Figure 1-3](#)).

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>AC Response</b>						
Gain Bandwidth Product	GBWP	—	5.0	—	MHz	
Phase Margin at Unity-Gain	PM	—	65	—	°	$G = +1\text{ V/V}$
Slew Rate	SR	—	2.5	—	V/ $\mu\text{s}$	
<b>Noise</b>						
Input Noise Voltage	$E_{ni}$	—	5.2	—	$\mu\text{V}_{P-P}$	$f = 0.1\text{ Hz to }10\text{ Hz}$
Input Noise Voltage Density	$e_{ni}$	—	16	—	nV/ $\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$
Input Noise Current Density	$i_{ni}$	—	3	—	fA/ $\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$

## MCP6283/MCP6285 CHIP SELECT ( $\overline{\text{CS}}$ ) SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.2\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_{CM} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$ ,  $C_L = 60\text{ pF}$  and  $\overline{\text{CS}}$  is tied low. (refer to [Figure 1-2](#) and [Figure 1-3](#)).

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>CS Low Specifications</b>						
$\overline{\text{CS}}$ Logic Threshold, Low	$V_{IL}$	$V_{SS}$	—	$0.2 V_{DD}$	V	
$\overline{\text{CS}}$ Input Current, Low	$I_{CSL}$	—	0.01	—	$\mu\text{A}$	$\overline{\text{CS}} = V_{SS}$
<b>CS High Specifications</b>						
$\overline{\text{CS}}$ Logic Threshold, High	$V_{IH}$	$0.8 V_{DD}$	—	$V_{DD}$	V	
$\overline{\text{CS}}$ Input Current, High	$I_{CSH}$	—	0.7	2	$\mu\text{A}$	$\overline{\text{CS}} = V_{DD}$
GND Current per Amplifier	$I_{SS}$	—	-0.7	—	$\mu\text{A}$	$\overline{\text{CS}} = V_{DD}$
Amplifier Output Leakage	—	—	0.01	—	$\mu\text{A}$	$\overline{\text{CS}} = V_{DD}$
<b>Dynamic Specifications (Note 1)</b>						
$\overline{\text{CS}}$ Low to Valid Amplifier Output, Turn-on Time	$t_{ON}$	—	4	10	$\mu\text{s}$	$\overline{\text{CS}} \text{ Low} \leq 0.2 V_{DD}$ , $G = +1\text{ V/V}$ , $V_{IN} = V_{DD}/2$ , $V_{OUT} = 0.9 V_{DD}/2$ , $V_{DD} = 5.0\text{V}$
$\overline{\text{CS}}$ High to Amplifier Output High-Z	$t_{OFF}$	—	0.01	—	$\mu\text{s}$	$\overline{\text{CS}} \text{ High} \geq 0.8 V_{DD}$ , $G = +1\text{ V/V}$ , $V_{IN} = V_{DD}/2$ , $V_{OUT} = 0.1 V_{DD}/2$
Hysteresis	$V_{HYST}$	—	0.6	—	V	$V_{DD} = 5\text{V}$

**Note 1:** The input condition ( $V_{IN}$ ) specified applies to both op amp A and B of the MCP6285. The dynamic specification is tested at the output of op amp B ( $V_{OUTB}$ ).



**FIGURE 1-1:** Timing Diagram for the Chip Select ( $\overline{\text{CS}}$ ) pin on the MCP6283 and MCP6285.

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## TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +2.2V$ to $+5.5V$ and $V_{SS} = GND$ .						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Operating Temperature Range	$T_A$	-40	—	+125	°C	Note
Storage Temperature Range	$T_A$	-65	—	+150	°C	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 5L-SOT-23	$\theta_{JA}$	—	256	—	°C/W	
Thermal Resistance, 6L-SOT-23	$\theta_{JA}$	—	230	—	°C/W	
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	$\theta_{JA}$	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	°C/W	

**Note:** The Junction Temperature ( $T_J$ ) must not exceed the Absolute Maximum specification of  $+150^\circ\text{C}$ .

### 1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in [Figure 1-2](#) and [Figure 1-2](#). The bypass capacitors are laid out according to the rules discussed in [Section 4.6 “Supply Bypass”](#).



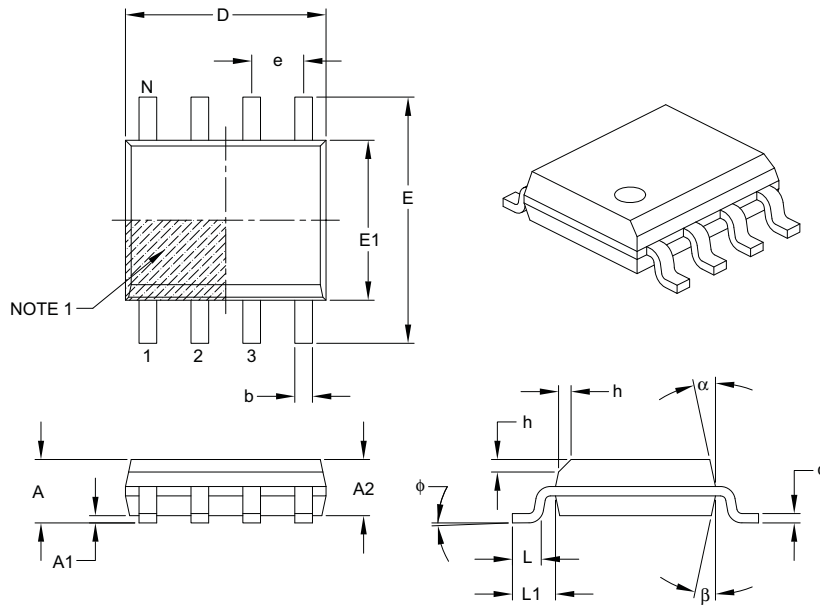
**FIGURE 1-2:** AC and DC Test Circuit for Most Non-Inverting Gain Conditions.



**FIGURE 1-3:** AC and DC Test Circuit for Most Inverting Gain Conditions.

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## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	$\phi$	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	$\alpha$	5°	–	15°
Mold Draft Angle Bottom	$\beta$	5°	–	15°

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

# MCP6281/1R/2/3/4/5

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	—	X	/XX	
Device		Temperature Range	Package	
Device:	MCP6281:		Single Op Amp	
	MCP6281T:		Single Op Amp (Tape and Reel) (SOIC, MSOP, SOT-23-5)	
	MCP6281RT:		Single Op Amp (Tape and Reel) (SOT-23-5)	
	MCP6282:		Dual Op Amp	
	MCP6282T:		Dual Op Amp (Tape and Reel) (SOIC, MSOP)	
	MCP6283:		Single Op Amp with $\overline{CS}$	
	MCP6283T:		Single Op Amp with $\overline{CS}$ (Tape and Reel) (SOIC, MSOP, SOT-23-6)	
	MCP6284:		Quad Op Amp	
	MCP6284T:		Quad Op Amp (Tape and Reel) (SOIC, TSSOP)	
	MCP6285:		Dual Op Amp with $\overline{CS}$	
	MCP6285T:		Dual Op Amp with $\overline{CS}$ (Tape and Reel) (SOIC, MSOP)	
Temperature Range:	E	=	-40°C to +125°C	
Package:	CH	=	Plastic Small Outline Transistor (SOT-23), 6-lead (MCP6283 only)	
	MS	=	Plastic MSOP, 8-lead	
	P	=	Plastic DIP (300 mil body), 8-lead, 14-lead	
	OT	=	Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6281, MCP6281R only)	
	SL	=	Plastic SOIC (3.90 mm body), 14-lead	
	SN	=	Plastic SOIC, (3.90 mm body), 8-lead	
	ST	=	Plastic TSSOP (4.4 mm body), 14-lead	
				<b>Examples:</b>
				a) MCP6281-E/SN: Extended Temperature, 8LD SOIC package.
				b) MCP6281-E/MS: Extended Temperature, 8LD MSOP package.
				c) MCP6281-E/P: Extended Temperature, 8LD PDIP package.
				d) MCP6281T-E/OT: Tape and Reel, Extended Temperature, 5LD SOT-23 package.
				e) MCP6281RT-E/OT: Tape and Reel, Extended Temperature, 5LD SOT-23 package.
				a) MCP6282-E/SN: Extended Temperature, 8LD SOIC package.
				b) MCP6282-E/MS: Extended Temperature, 8LD MSOP package.
				c) MCP6282-E/P: Extended Temperature, 8LD PDIP package.
				d) MCP6282T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC package.
				a) MCP6283-E/SN: Extended Temperature, 8LD SOIC package.
				b) MCP6283-E/MS: Extended Temperature, 8LD MSOP package.
				c) MCP6283-E/P: Extended Temperature, 8LD PDIP package.
				d) MCP6283T-E/CH: Tape and Reel, Extended Temperature, 6LD SOT-23 package.
				a) MCP6284-E/P: Extended Temperature, 14LD PDIP package.
				b) MCP6284T-E/SL: Tape and Reel, Extended Temperature, 14LD SOIC package.
				c) MCP6284-E/SL: Extended Temperature, 14LD SOIC package.
				d) MCP6284-E/ST: Extended Temperature, 14LD TSSOP package.
				a) MCP6285-E/SN: Extended Temperature, 8LD SOIC package.
				b) MCP6285-E/MS: Extended Temperature, 8LD MSOP package.
				c) MCP6285-E/P: Extended Temperature, 8LD PDIP package.
				d) MCP6285T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC package.