# PIC24FJ128GA FAMILY

## General Purpose, 16-bit Flash Microcontrollers

### High-Performance CPU:

- Modified Harvard Architecture
- Up to 16 MIPS operation @ 32 MHz
- 8 MHz internal oscillator:
  - 4x PLL option
  - Multiple divide options
- 17-bit x 17-bit Single-Cycle Hardware Fractional/Integer Multiplier
- 32-bit by 16-bit Hardware Divider
- 16 x 16-bit Working Register Array
- C compiler Optimized Instruction Set Architecture:
  - 76 base instructions
  - Flexible addressing modes
- Linear Program Memory Addressing up to 12 Mbytes
- Linear Data Memory Addressing up to 64 Kbytes
- Two Address Generation Units for separate Read and Write Addressing of Data Memory

### Special Microcontroller Features:

- Operating Voltage Range of 2.0V to 3.6V
- Flash Program Memory:
  - 1000 erase/write cycles, typical
  - Flash retention 20 years, typical
- Self-Reprogrammable under Software Control
- Selectable Power Management modes:
  - Sleep, Idle and Alternate Clock modes
- Fail-Safe Clock Monitor operation:
  - Detects clock failure and switches to on-chip, low-power RC oscillator
- On-Chip LDO Regulator
- JTAG Boundary Scan and Programming Support
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with On-Chip, Low-Power RC Oscillator for reliable operation
- In-Circuit Serial Programming™ (ICSP™) and In-Circuit Emulation (ICE) via 2 pins

### Analog Features:

- 10-bit, up to 16-channel Analog-to-Digital Converter (A/D):
  - 500 ksps conversion rate
  - Conversion available during Sleep and Idle
- Dual Analog Comparators with Programmable Input/Output Configuration

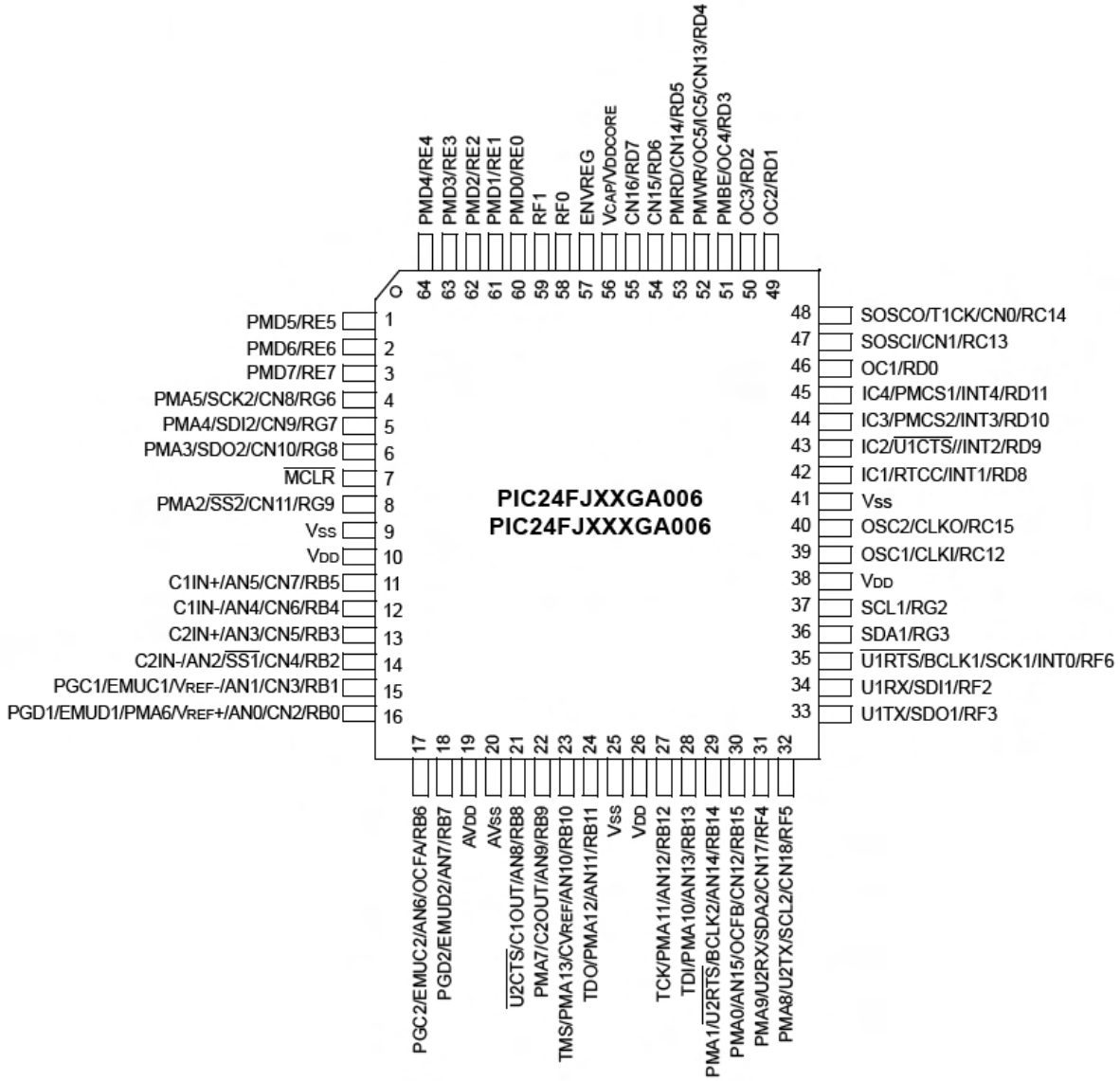
### Peripheral Features:

- Two 3-wire/4-wire SPI modules, supporting 4 Frame modes with 4-level FIFO Buffer
- Two $I^2C$™ modules support Multi-Master/Slave mode and 7-bit/10-bit Addressing
- Two UART modules:
  - Supports RS-232, RS-485 and LIN 1.2
  - Supports IrDA® with on-chip hardware endec
  - Auto-Wake-up on Start bit
  - Auto-Baud Detect
  - 4-level FIFO buffer
- Parallel Master Slave Port (PMP/PSP):
  - Supports 8-bit or 16-bit data
  - Supports 16 address lines
- Hardware Real-Time Clock/Calendar (RTCC):
  - Provides clock, calendar and alarm functions
- Five 16-bit Timers/Counters with Programmable prescaler
- Five 16-bit Capture Inputs
- Five 16-bit Compare/PWM Outputs
- High-Current Sink/Source on select I/O pins: 18 mA/18 mA
- Configurable Open-Drain Output on Digital I/O pins
- Up to 5 External Interrupt Sources

| Device | Pins | Program Memory (Bytes) | SRAM (Bytes) | Timers 16-bit | Capture Input | Compare/ PWM Output | UART | SPI | $I^2C$™ | 10-bit A/D (ch) | Comparators | PMP/PSP | JTAG |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PIC24FJ64GA006 | 64 | 64K | 8K | 5 | 5 | 5 | 2 | 2 | 2 | 16 | 2 | Y | Y |
| PIC24FJ96GA006 | 64 | 96K | 8K | 5 | 5 | 5 | 2 | 2 | 2 | 16 | 2 | Y | Y |
| PIC24FJ128GA006 | 64 | 128K | 8K | 5 | 5 | 5 | 2 | 2 | 2 | 16 | 2 | Y | Y |
| PIC24FJ64GA008 | 80 | 64K | 8K | 5 | 5 | 5 | 2 | 2 | 2 | 16 | 2 | Y | Y |
| PIC24FJ96GA008 | 80 | 96K | 8K | 5 | 5 | 5 | 2 | 2 | 2 | 16 | 2 | Y | Y |
| PIC24FJ128GA008 | 80 | 128K | 8K | 5 | 5 | 5 | 2 | 2 | 2 | 16 | 2 | Y | Y |
| PIC24FJ64GA010 | 100 | 64K | 8K | 5 | 5 | 5 | 2 | 2 | 2 | 16 | 2 | Y | Y |
| PIC24FJ96GA010 | 100 | 96K | 8K | 5 | 5 | 5 | 2 | 2 | 2 | 16 | 2 | Y | Y |
| PIC24FJ128GA010 | 100 | 128K | 8K | 5 | 5 | 5 | 2 | 2 | 2 | 16 | 2 | Y | Y |

## Pin Diagrams

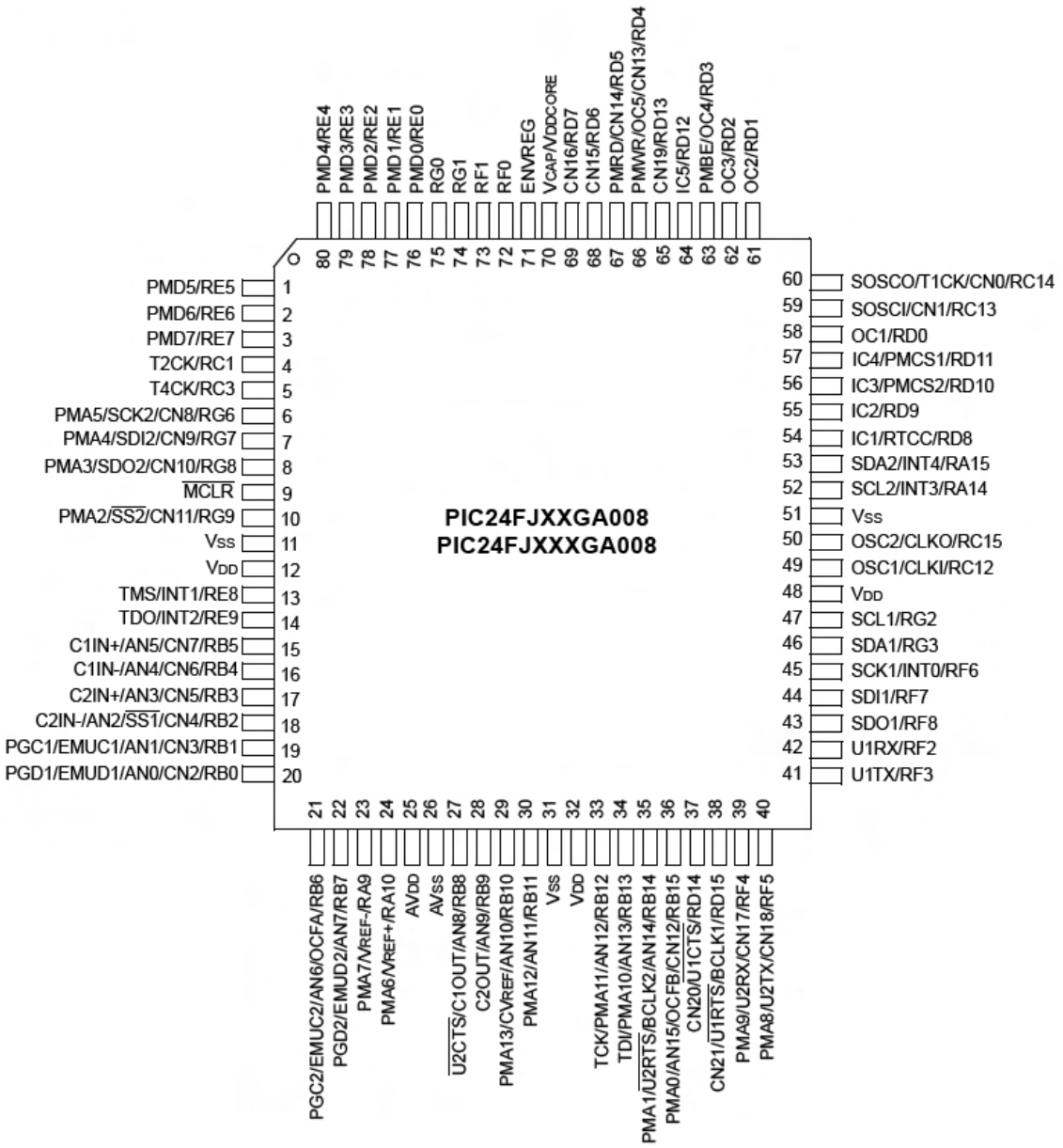
**64-Pin TQFP**



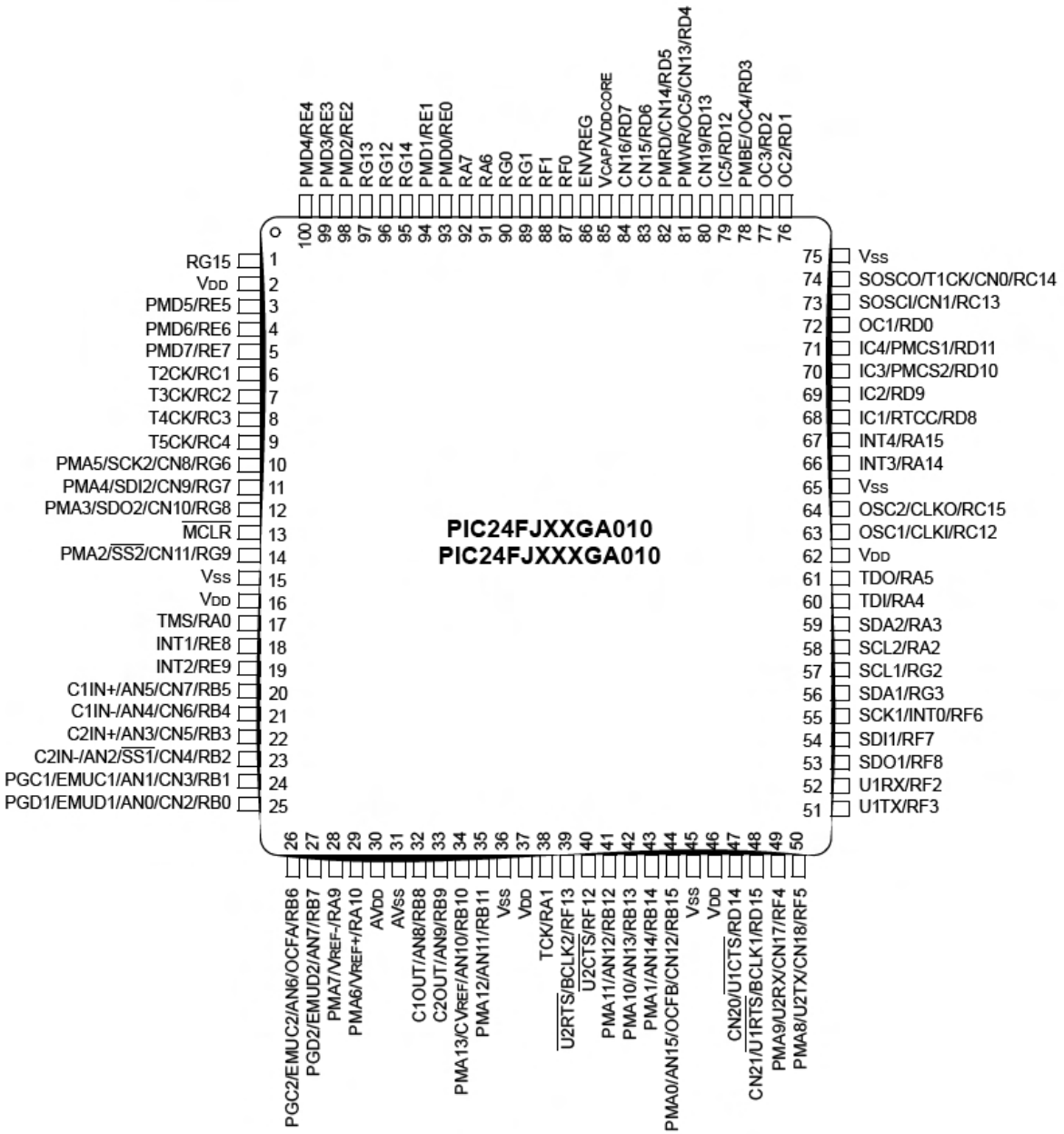
## Pin Diagrams (Continued)

**80-Pin TQFP**



## Pin Diagrams (Continued))

**100-Pin TQFP**



# 1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC24FJ64GA006
- PIC24FJ64GA008
- PIC24FJ64GA010
- PIC24FJ96GA006
- PIC24FJ96GA008
- PIC24FJ96GA010
- PIC24FJ128GA006
- PIC24FJ128GA008
- PIC24FJ128GA010

This family introduces a new line of Microchip devices: a 16-bit RISC microcontroller family with a broad peripheral feature set and enhanced computational performance. The PIC24FJ128GA family offers a new migration option for those high-performance applications which may be outgrowing their 8-bit platforms, but don't require the numerical processing power of a digital signal processor.

## 1.1 Core Features

### 1.1.1 16-BIT ARCHITECTURE

Central to all PIC24 devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC® digital signal controllers. The PIC24 CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths, with the ability to move information between data and memory spaces
- Linear addressing of up to 8 Mbytes (program space) and 64 Kbytes (data)
- A 16-element working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages such as 'C'
- Operational performance up to 16 MIPS

### 1.1.2 POWER-SAVING TECHNOLOGY

All of the devices in the PIC24FJ128GA family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **On-the-Fly Clock Switching:** The device clock can be changed under software control to the Timer1 source or the internal low-power RC oscillator during operation, allowing the user to incorporate power-saving ideas into their software designs.
- **Doze Mode Operation:** When timing-sensitive applications, such as serial communications, require the uninterrupted operation of peripherals, the CPU clock speed can be selectively reduced, allowing incremental power savings without missing a beat.
- **Instruction-Based Power-Saving Modes:** The microcontroller can suspend all operations, or selectively shut down its core while leaving its peripherals active, with a single instruction in software.

### 1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ128GA family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of a divide-by-2 clock output.
- A Fast Internal Oscillator (FRC) with a nominal 8 MHz output, which can also be divided under software control to provide clock speeds as low as 31 kHz.
- A Phase Lock Loop (PLL) frequency multiplier, available to the external oscillator modes and the FRC oscillator, which allows clock speeds of up to 32 MHz.
- A separate internal RC oscillator (LPRC) with a fixed 31 kHz output, which provides a low-power option for timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor. This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

### 1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device. This is true when moving between devices with the same pin count, or even jumping from 64-pin to 80-pin to 100-pin devices.

The PIC24 family is pin-compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple to the powerful and complex, yet still select a Microchip device.

## 1.2 Other Special Features

- **Communications:** The PIC24FJ128GA family incorporates a range of serial communication peripherals to handle a range of application requirements. All devices are equipped with two independent UARTs with built-in IrDA encoder/decoders. There are also two independent SPI modules, and two independent $I^2C$ modules that support both Master and Slave modes of operation.
- **Parallel Master/Enhanced Parallel Slave Port:** One of the general purpose I/O ports can be reconfigured for enhanced parallel data communications. In this mode, the port can be configured for both master and slave operations, and supports 8-bit and 16-bit data transfers with up to 16 external address lines in Master modes.
- **Real-Time Clock/Calendar:** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, as well as faster sampling speeds.

## 1.3 Details on Individual Family Members

Devices in the PIC24FJ128GA family are available in 64-pin, 80-pin and 100-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in two ways:

1. Flash program memory (64 Kbytes for PIC24FJ64GA devices, 96 Kbytes for PIC24FJ96GA devices and 128 Kbytes for PIC24FJ128GA devices).
2. Available I/O pins and ports (53 pins on 6 ports for 64-pin devices, 69 pins on 7 ports for 80-pin devices and 84 pins on 7 ports for 100-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1.

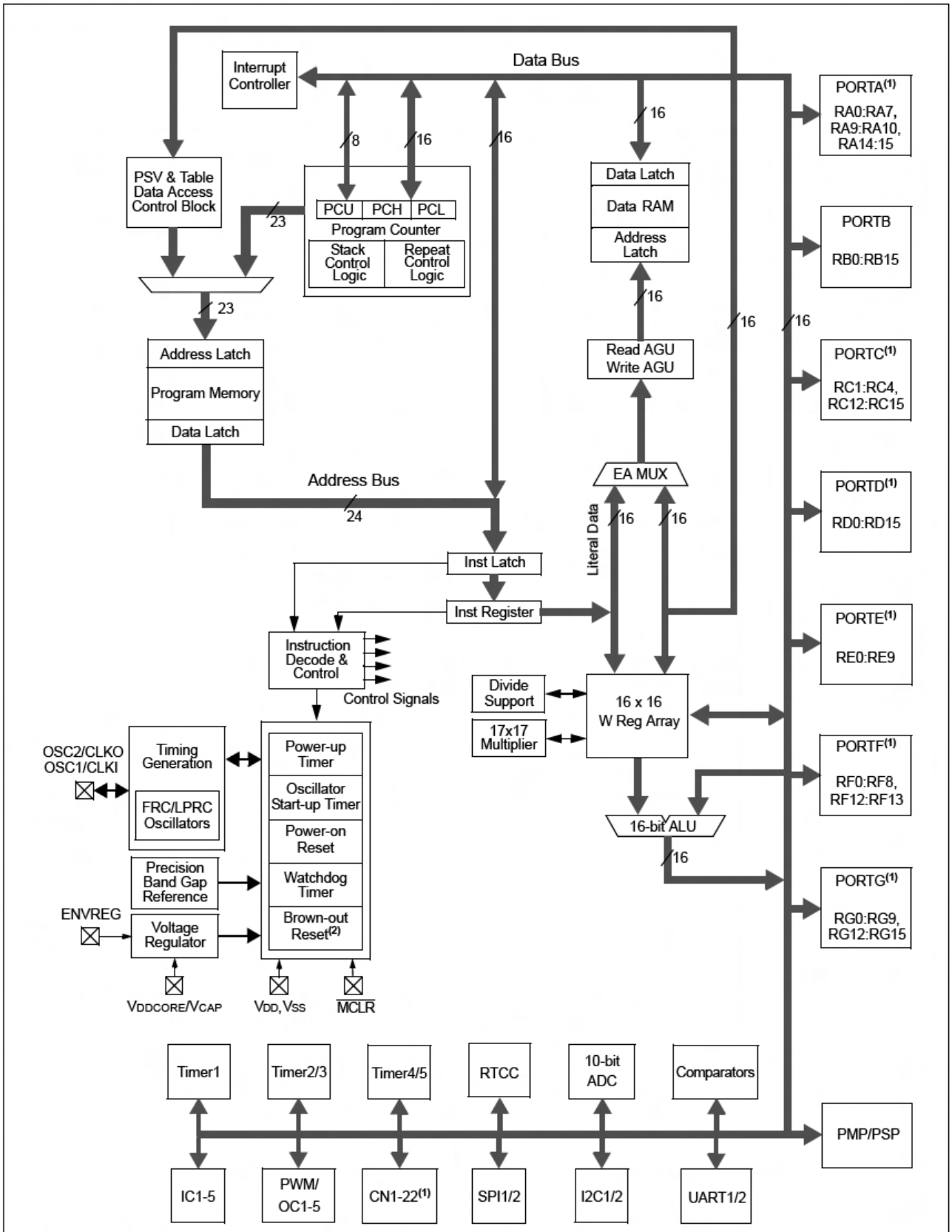
A list of the pin features available on the PIC24FJ128GA family devices, sorted by function, is shown in Table 1-2. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of the data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

**TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ128GA FAMILY**

| Features | PIC24FJ64GA006 | PIC24FJ96GA006 | PIC24FJ128GA006 | PIC24FJ64GA008 | PIC24FJ96GA008 | PIC24FJ128GA008 | PIC24FJ64GA010 | PIC24FJ96GA010 | PIC24FJ128GA010 |
|---|---|---|---|---|---|---|---|---|---|
| Operating Frequency | DC – 32 MHz | | | | | | | | |
| Program Memory (Bytes) | 64K | 96K | 128K | 64K | 96K | 128K | 64K | 96K | 128K |
| Program Memory (Instructions) | 22,016 | 32,768 | 44,032 | 22,016 | 32,768 | 44,032 | 22,016 | 32,768 | 44,032 |
| Data Memory (Bytes) | 8192 | | | | | | | | |
| Interrupt Sources (Soft Vectors/NMI Traps) | 43 (39/4) | | | | | | | | |
| I/O Ports | Ports B, C, D, E, F, G | | | Ports A, B, C, D, E, F, G | | | Ports A, B, C, D, E, F, G | | |
| Total I/O Pins | 53 | | | 69 | | | 84 | | |
| Timers: | | | | | | | | | |
| Total number (16-bit) | 5 | | | | | | | | |
| 32-bit (from paired 16-bit timers) | 2 | | | | | | | | |
| Input Capture Channels | 5 | | | | | | | | |
| Output Compare/PWM Channels | 5 | | | | | | | | |
| Input Change Notification Interrupt | 19 | | | 22 | | | | | |
| Serial Communications: | | | | | | | | | |
| Enhanced UART | 2 | | | | | | | | |
| SPI (3-wire/4-wire) | 2 | | | | | | | | |
| $I^2C$™ | 2 | | | | | | | | |
| Parallel Communications (PMP/PSP) | Yes | | | | | | | | |
| JTAG Boundary Scan | Yes | | | | | | | | |
| 10-bit Analog-to-Digital Module (input channels) | 16 | | | | | | | | |
| Analog Comparators | 2 | | | | | | | | |
| Resets (and Delays) | POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT; Illegal Opcode, Repeat Hardware Traps, (PWRT, OST, PLL Lock) | | | | | | | | |
| Instruction Set | 76 Base Instructions, Multiple Addressing Mode Variations | | | | | | | | |
| Packages | 64-pin TQFP | | | 80-pin TQFP | | | 100-pin TQFP | | |

**FIGURE 1-1: PIC24FJ128GA FAMILY GENERAL BLOCK DIAGRAM**




**Note 1:** Not all pins or features are implemented on all device pinout configurations. See Table 1-2 for I/O port pin descriptions.

**2:** BOR functionality is provided when the on-board voltage regulator is enabled.

**TABLE 1-2: PIC24FJ128GA FAMILY PINOUT DESCRIPTIONS**

| Function | Pin Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-pin | 80-pin | 100-pin | | | |
| AN0 | 16 | 20 | 25 | I | ANA | A/D Analog Inputs. |
| AN1 | 15 | 19 | 24 | I | ANA | |
| AN2 | 14 | 18 | 23 | I | ANA | |
| AN3 | 13 | 17 | 22 | I | ANA | |
| AN4 | 12 | 16 | 21 | I | ANA | |
| AN5 | 11 | 15 | 20 | I | ANA | |
| AN6 | 17 | 21 | 26 | I | ANA | |
| AN7 | 18 | 22 | 27 | I | ANA | |
| AN8 | 21 | 27 | 32 | I | ANA | |
| AN9 | 22 | 28 | 33 | I | ANA | |
| AN10 | 23 | 29 | 34 | I | ANA | |
| AN11 | 24 | 30 | 35 | I | ANA | |
| AN12 | 27 | 33 | 41 | I | ANA | |
| AN13 | 28 | 34 | 42 | I | ANA | |
| AN14 | 29 | 35 | 43 | I | ANA | |
| AN15 | 30 | 36 | 44 | I | ANA | |
| AVDD | 19 | 25 | 30 | P | — | Positive Supply for Analog Modules. |
| AVSS | 20 | 26 | 31 | P | — | Ground Reference for Analog Modules. |
| BCLK1 | 35 | 38 | 48 | O | — | UART1 IrDA® Baud Clock. |
| BCLK2 | 29 | 35 | 39 | O | — | UART2 IrDA® Baud Clock. |
| C1IN- | 12 | 16 | 21 | I | ANA | Comparator 1 Negative Input. |
| C1IN+ | 11 | 15 | 20 | I | ANA | Comparator 1 Positive Input. |
| C1OUT | 21 | 27 | 32 | O | — | Comparator 1 Output. |
| C2IN- | 14 | 18 | 23 | I | ANA | Comparator 2 Negative Input. |
| C2IN+ | 13 | 17 | 22 | I | ANA | Comparator 2 Positive Input. |
| C2OUT | 22 | 28 | 33 | O | — | Comparator 2 Output. |
| CLKI | 39 | 49 | 63 | I | ANA | Main Clock Input Connection. |
| CLKO | 40 | 50 | 64 | O | — | System Clock Output. |
| CN0 | 48 | 60 | 74 | I | ST | Interrupt-on-Change Inputs. |
| CN1 | 47 | 59 | 73 | I | ST | |
| CN2 | 16 | 20 | 25 | I | ST | |
| CN3 | 15 | 19 | 24 | I | ST | |
| CN4 | 14 | 18 | 23 | I | ST | |
| CN5 | 13 | 17 | 22 | I | ST | |
| CN6 | 12 | 16 | 21 | I | ST | |
| CN7 | 11 | 15 | 20 | I | ST | |
| CN8 | 4 | 6 | 10 | I | ST | |
| CN9 | 5 | 7 | 11 | I | ST | |
| CN10 | 6 | 8 | 12 | I | ST | |
| CN11 | 8 | 10 | 14 | I | ST | |
| CN12 | 30 | 36 | 44 | I | ST | |
| CN13 | 52 | 66 | 81 | I | ST | |
| CN14 | 53 | 67 | 82 | I | ST | |
| CN15 | 54 | 68 | 83 | I | ST | |
| CN16 | 55 | 69 | 84 | I | ST | |
| CN17 | 31 | 39 | 49 | I | ST | |

**Legend:** TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
$I^2C$™ = $I^2C$/SMBus input buffer

**TABLE 1-2: PIC24FJ128GA FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

| Function | Pin Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-pin | 80-pin | 100-pin | | | |
| CN18 | 32 | 40 | 50 | I | ST | Interrupt-on-Change Inputs. |
| CN19 | — | 65 | 80 | I | ST | |
| CN20 | — | 37 | 47 | I | ST | |
| CN21 | — | 38 | 48 | I | ST | |
| CVREF | 23 | 29 | 34 | O | ANA | Comparator Voltage Reference Output. |
| EMUC1 | 15 | 19 | 24 | I/O | ST | In-Circuit Emulator Clock Input/Output. |
| EMUD1 | 16 | 20 | 25 | I/O | ST | In-Circuit Emulator Data Input/Output. |
| EMUC2 | 17 | 21 | 26 | I/O | ST | In-Circuit Emulator Clock Input/Output. |
| EMUD2 | 18 | 22 | 27 | I/O | ST | In-Circuit Emulator Data Input/Output. |
| ENVREG | 57 | 71 | 86 | I | ST | Enable for On-Chip Voltage Regulator. |
| IC1 | 42 | 54 | 68 | I | ST | Input Capture Inputs. |
| IC2 | 43 | 55 | 69 | I | ST | |
| IC3 | 44 | 56 | 70 | I | ST | |
| IC4 | 45 | 57 | 71 | I | ST | |
| IC5 | 52 | 64 | 79 | I | ST | |
| INT0 | 35 | 45 | 55 | I | ST | External Interrupt Inputs. |
| INT1 | 42 | 13 | 18 | I | ST | |
| INT2 | 43 | 14 | 19 | I | ST | |
| INT3 | 44 | 52 | 66 | I | ST | |
| INT4 | 45 | 53 | 67 | I | ST | |
| $\overline{MCLR}$ | 7 | 9 | 13 | I | ST | Master Clear (Device Reset) Input. This line is brought low to cause a Reset. |
| OC1 | 46 | 58 | 72 | O | — | Output Compare/PWM Outputs. |
| OC2 | 49 | 61 | 76 | O | — | |
| OC3 | 50 | 62 | 77 | O | — | |
| OC4 | 51 | 63 | 78 | O | — | |
| OC5 | 52 | 66 | 81 | O | — | |
| OCFA | 17 | 21 | 26 | I | ST | Output Compare Fault A Input. |
| OCFB | 30 | 36 | 44 | I | ST | Output Compare Fault B Input. |
| OSC1 | 39 | 49 | 63 | I | ANA | Main Oscillator Input Connection. |
| OSC2 | 40 | 50 | 64 | O | ANA | Main Oscillator Output Connection. |
| PGC1 | 15 | 19 | 24 | I/O | ST | In-Circuit Debugger and ICSP™ Programming Clock |
| PGD1 | 16 | 20 | 25 | I/O | ST | In-Circuit Debugger and ICSP Programming Data. |
| PGC2 | 17 | 21 | 26 | I/O | ST | In-Circuit Debugger and ICSP™ Programming Clock. |
| PGD2 | 18 | 22 | 27 | I/O | ST | In-Circuit Debugger and ICSP Programming Data. |

**Legend:** TTL = TTL input buffer
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$I^2C$™ = $I^2C$/SMBus input buffer

 

**TABLE 1-2: PIC24FJ128GA FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

| Function | Pin Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-pin | 80-pin | 100-pin | | | |
| PMA0 | 30 | 36 | 44 | I/O | ST | Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes). |
| PMA1 | 29 | 35 | 43 | I/O | ST | Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes). |
| PMA2 | 8 | 10 | 14 | O | — | Parallel Master Port Address (Demultiplexed Master modes). |
| PMA3 | 6 | 8 | 12 | O | — | |
| PMA4 | 5 | 7 | 11 | O | — | |
| PMA5 | 4 | 6 | 10 | O | — | |
| PMA6 | 16 | 24 | 29 | O | — | |
| PMA7 | 22 | 23 | 28 | O | — | |
| PMA8 | 32 | 40 | 50 | O | — | |
| PMA9 | 31 | 39 | 49 | O | — | |
| PMA10 | 28 | 34 | 42 | O | — | |
| PMA11 | 27 | 33 | 41 | O | — | |
| PMA12 | 24 | 30 | 35 | O | — | |
| PMA13 | 23 | 29 | 34 | O | — | |
| PMBE | 51 | 63 | 78 | O | — | Parallel Master Port Byte Enable Strobe. |
| PMCS1 | 45 | 57 | 71 | O | — | Parallel Master Port Chip Select 1 Strobe/Address bit 14. |
| PMCS2 | 44 | 56 | 70 | O | — | Parallel Master Port Chip Select 2 Strobe/Address bit 15. |
| PMD0 | 60 | 76 | 93 | I/O | ST | Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes). |
| PMD1 | 61 | 77 | 94 | I/O | ST | |
| PMD2 | 62 | 78 | 98 | I/O | ST | |
| PMD3 | 63 | 79 | 99 | I/O | ST | |
| PMD4 | 64 | 80 | 100 | I/O | ST | |
| PMD5 | 1 | 1 | 3 | I/O | ST | |
| PMD6 | 2 | 2 | 4 | I/O | ST | |
| PMD7 | 3 | 3 | 5 | I/O | ST | |
| PMRD | 53 | 67 | 82 | O | — | Parallel Master Port Read Strobe. |
| PMWR | 52 | 66 | 81 | O | — | Parallel Master Port Write Strobe. |

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**TABLE 1-2: PIC24FJ128GA FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

| Function | Pin Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-pin | 80-pin | 100-pin | | | |
| RA0 | — | — | 17 | I/O | ST | PORTA Digital I/O. |
| RA1 | — | — | 38 | I/O | ST | |
| RA2 | — | — | 58 | I/O | ST | |
| RA3 | — | — | 59 | I/O | ST | |
| RA4 | — | — | 60 | I/O | ST | |
| RA5 | — | — | 61 | I/O | ST | |
| RA6 | — | — | 91 | I/O | ST | |
| RA7 | — | — | 92 | I/O | ST | |
| RA9 | — | 23 | 28 | I/O | ST | |
| RA10 | — | 24 | 29 | I/O | ST | |
| RA14 | — | 52 | 66 | I/O | ST | |
| RA15 | — | 53 | 67 | I/O | ST | |
| RB0 | 16 | 20 | 25 | I/O | ST | PORTB Digital I/O. |
| RB1 | 15 | 19 | 24 | I/O | ST | |
| RB2 | 14 | 18 | 23 | I/O | ST | |
| RB3 | 13 | 17 | 22 | I/O | ST | |
| RB4 | 12 | 16 | 21 | I/O | ST | |
| RB5 | 11 | 15 | 20 | I/O | ST | |
| RB6 | 17 | 21 | 26 | I/O | ST | |
| RB7 | 18 | 22 | 27 | I/O | ST | |
| RB8 | 21 | 27 | 32 | I/O | ST | |
| RB9 | 22 | 28 | 33 | I/O | ST | |
| RB10 | 23 | 29 | 34 | I/O | ST | |
| RB11 | 24 | 30 | 35 | I/O | ST | |
| RB12 | 27 | 33 | 41 | I/O | ST | |
| RB13 | 28 | 34 | 42 | I/O | ST | |
| RB14 | 29 | 35 | 43 | I/O | ST | |
| RB15 | 30 | 36 | 44 | I/O | ST | |
| RC1 | — | 4 | 6 | I/O | ST | PORTC Digital I/O. |
| RC2 | — | — | 7 | I/O | ST | |
| RC3 | — | 5 | 8 | I/O | ST | |
| RC4 | — | — | 9 | I/O | ST | |
| RC12 | 39 | 49 | 63 | I/O | ST | |
| RC13 | 47 | 59 | 73 | I/O | ST | |
| RC14 | 48 | 60 | 74 | I/O | ST | |
| RC15 | 40 | 50 | 64 | I/O | ST | |

**Legend:** TTL = TTL input buffer
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**TABLE 1-2: PIC24FJ128GA FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

| Function | Pin Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-pin | 80-pin | 100-pin | | | |
| RD0 | 46 | 58 | 72 | I/O | ST | PORTD Digital I/O. |
| RD1 | 49 | 61 | 76 | I/O | ST | |
| RD2 | 50 | 62 | 77 | I/O | ST | |
| RD3 | 51 | 63 | 78 | I/O | ST | |
| RD4 | 52 | 66 | 81 | I/O | ST | |
| RD5 | 53 | 67 | 82 | I/O | ST | |
| RD6 | 54 | 68 | 83 | I/O | ST | |
| RD7 | 55 | 69 | 84 | I/O | ST | |
| RD8 | 42 | 54 | 68 | I/O | ST | |
| RD9 | 43 | 55 | 69 | I/O | ST | |
| RD10 | 44 | 56 | 70 | I/O | ST | |
| RD11 | 45 | 57 | 71 | I/O | ST | |
| RD12 | — | 64 | 79 | I/O | ST | |
| RD13 | — | 65 | 80 | I/O | ST | |
| RD14 | — | 37 | 47 | I/O | ST | |
| RD15 | — | 38 | 48 | I/O | ST | |
| RE0 | 60 | 76 | 93 | I/O | ST | PORTE Digital I/O. |
| RE1 | 61 | 77 | 94 | I/O | ST | |
| RE2 | 62 | 78 | 98 | I/O | ST | |
| RE3 | 63 | 79 | 99 | I/O | ST | |
| RE4 | 64 | 80 | 100 | I/O | ST | |
| RE5 | 1 | 1 | 3 | I/O | ST | |
| RE6 | 2 | 2 | 4 | I/O | ST | |
| RE7 | 3 | 3 | 5 | I/O | ST | |
| RE8 | — | 13 | 18 | I/O | ST | |
| RE9 | — | 14 | 19 | I/O | ST | |
| RF0 | 58 | 72 | 87 | I/O | ST | PORTF Digital I/O. |
| RF1 | 59 | 73 | 88 | I/O | ST | |
| RF2 | 34 | 42 | 52 | I/O | ST | |
| RF3 | 33 | 41 | 51 | I/O | ST | |
| RF4 | 31 | 39 | 49 | I/O | ST | |
| RF5 | 32 | 40 | 50 | I/O | ST | |
| RF6 | 35 | 45 | 55 | I/O | ST | |
| RF7 | — | 44 | 54 | I/O | ST | |
| RF8 | — | 43 | 53 | I/O | ST | |
| RF12 | — | — | 40 | I/O | ST | |
| RF13 | — | — | 39 | I/O | ST | |

**Legend:** TTL = TTL input buffer
ANA = Analog level input/output
ST = Schmitt Trigger input buffer
$I^2C$™ = $I^2C$/SMBus input buffer

**TABLE 1-2: PIC24FJ128GA FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

| Function | Pin Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-pin | 80-pin | 100-pin | | | |
| RG0 | — | 75 | 90 | I/O | ST | PORTG Digital I/O. |
| RG1 | — | 74 | 89 | I/O | ST | |
| RG2 | 37 | 47 | 57 | I/O | ST | |
| RG3 | 36 | 46 | 56 | I/O | ST | |
| RG6 | 4 | 6 | 10 | I/O | ST | |
| RG7 | 5 | 7 | 11 | I/O | ST | |
| RG8 | 6 | 8 | 12 | I/O | ST | |
| RG9 | 8 | 10 | 14 | I/O | ST | |
| RG12 | — | — | 96 | I/O | ST | |
| RG13 | — | — | 97 | I/O | ST | |
| RG14 | — | — | 95 | I/O | ST | |
| RG15 | — | — | 1 | I/O | ST | |
| RTCC | 42 | 54 | 68 | O | — | Real-Time Clock Alarm Output. |
| SCK1 | 35 | 45 | 55 | O | — | SPI1 Serial Clock Output. |
| SCK2 | 4 | 6 | 10 | I/O | ST | SPI2 Serial Clock Output. |
| SCL1 | 37 | 47 | 57 | I/O | $I^2C$ | I2C1 Synchronous Serial Clock Input/Output. |
| SCL2 | 32 | 52 | 58 | I/O | $I^2C$ | I2C2 Synchronous Serial Clock Input/Output. |
| SDA1 | 36 | 46 | 56 | I/O | $I^2C$ | I2C1 Data Input/Output. |
| SDA2 | 31 | 53 | 59 | I/O | $I^2C$ | I2C2 Data Input/Output. |
| SDI1 | 34 | 44 | 54 | I | ST | SPI1 Serial Data Input. |
| SDI2 | 5 | 7 | 11 | I | ST | SPI2 Serial Data Input. |
| SDO1 | 33 | 43 | 53 | O | — | SPI1 Serial Data Output. |
| SDO2 | 6 | 8 | 12 | O | — | SPI2 Serial Data Output. |
| SOSCI | 47 | 59 | 73 | I | ANA | Secondary Oscillator/Timer1 Clock Input. |
| SOSCO | 48 | 60 | 74 | O | ANA | Secondary Oscillator/Timer1 Clock Output. |
| $\overline{SS1}$ | 14 | 18 | 23 | I/O | ST | Slave Select Input/Frame Select Output (SPI1). |
| $\overline{SS2}$ | 8 | 10 | 14 | I/O | ST | Slave Select Input/Frame Select Output (SPI2). |
| T1CK | 48 | 60 | 74 | I | ST | Timer1 Clock. |
| T2CK | — | 4 | 6 | I | ST | Timer2 External Clock Input. |
| T3CK | — | — | 7 | I | ST | Timer3 External Clock Input. |
| T4CK | — | 5 | 8 | I | ST | Timer4 External Clock Input. |
| T5CK | — | — | 9 | I | ST | Timer5 External Clock Input. |
| TCK | 27 | 33 | 38 | I | ST | JTAG Test Clock/Programming Clock Input. |
| TDI | 28 | 34 | 60 | I | ST | JTAG Test Data/Programming Data Input. |
| TDO | 24 | 14 | 61 | O | — | JTAG Test Data Output. |
| TMS | 23 | 13 | 17 | I | ST | JTAG Test Mode Select Input. |

**Legend:** TTL = TTL input buffer ST = Schmitt Trigger input buffer
ANA = Analog level input/output $I^2C$™ = $I^2C$/SMBus input buffer

 

**TABLE 1-2: PIC24FJ128GA FAMILY PINOUT DESCRIPTIONS (CONTINUED)**

| Function | Pin Number | | | I/O | Input Buffer | Description |
|---|---|---|---|---|---|---|
| | 64-pin | 80-pin | 100-pin | | | |
| $\overline{U1CTS}$ | 43 | 37 | 47 | I | ST | UART1 Clear to Send Input. |
| $\overline{U1RTS}$ | 35 | 38 | 48 | O | — | UART1 Request to Send Output. |
| U1RX | 34 | 42 | 52 | I | ST | UART1 Receive. |
| U1TX | 33 | 41 | 51 | O | DIG | UART1 Transmit Output. |
| $\overline{U2CTS}$ | 21 | 27 | 40 | I | ST | UART2 Clear to Send Input. |
| $\overline{U2RTS}$ | 29 | 35 | 39 | O | — | UART2 Request to Send Output. |
| U2RX | 31 | 39 | 49 | I | ST | UART 2 Receive Input. |
| U2TX | 32 | 40 | 50 | O | — | UART2 Transmit Output. |
| VDD | 10, 26, 38 | 12, 32, 48 | 2, 16, 37, 46, 62 | P | — | Positive Supply for Peripheral Digital Logic and I/O pins. |
| VDDCAP | 56 | 70 | 85 | P | — | External Filter Capacitor Connection (regulator enabled). |
| VDDCORE | 56 | 70 | 85 | P | — | Positive Supply for Microcontroller Core Logic (regulator disabled). |
| VREF- | 15 | 23 | 28 | I | ANA | A/D and Comparator Reference Voltage (Low) Input. |
| VREF+ | 16 | 24 | 29 | I | ANA | A/D and Comparator Reference Voltage (High) Input. |
| VSS | 9, 25, 41 | 11, 31, 51 | 15, 36, 45, 65, 75 | P | — | Ground Reference for Logic and I/O pins. |

**Legend:** TTL = TTL input buffer ST = Schmitt Trigger input buffer
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