

MCP1726

1A, Low Voltage, Low Quiescent Current LDO Regulator

Features

- 1A Output Current Capability
- Input Operating Voltage Range: 2.3V to 6.0V
- · Adjustable Output Voltage Range: 0.8V to 5.0V
- · Standard Fixed Output Voltages:
 - 0.8V, 1.2V, 1.8V, 2.5V, 3.3V, 5.0V
- · Low Dropout Voltage: 220 mV Typical at 1A
- Typical Output Voltage Tolerance: 0.4%
- Stable with 1.0 µF Ceramic Output Capacitor
- · Fast response to Load Transients
- Low Supply Current: 140 μA (typ)
- Low Shutdown Supply Current: 0.1 μA (typ)
- · Adjustable Delay on Power Good Output
- Short Circuit Current Limiting and Overtemperature Protection
- · 3x3 DFN-8 and SOIC-8 Package Options

Applications

- · High-Speed Driver Chipset Power
- · Networking Backplane Cards
- Notebook Computers
- · Network Interface Cards
- · Palmtop Computers
- · 2.5V to 1.XV Regulators

Description

The MCP1726 is a 1A Low Dropout (LDO) linear regulator that provides high current and low output voltages in a very small package. The MCP1726 comes in a fixed (or adjustable) output voltage version, with an output voltage range of 0.8V to 5.0V. The 1A output current capability, combined with the low output voltage capability, make the MCP1726 a good choice for new sub-1.8V output voltage LDO applications that have high current demands.

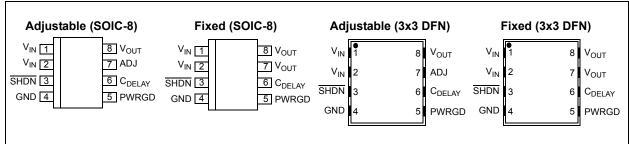
The MCP1726 is stable using ceramic output capacitors that inherently provide lower output noise and reduce the size and cost of the entire regulator solution. Only 1 μF of output capacitance is needed to stabilize the LDO.

Using CMOS construction, the quiescent current consumed by the MCP1726 is typically less than 140 μ A over the entire input voltage range, making it attractive for portable computing applications that demand high output current. When shut down, the quiescent current is reduced to less than 0.1 μ A.

The scaled-down output voltage is internally monitored and a power good (PWRGD) output is provided when the output is within 92% of regulation (typical). An external capacitor can be used on the C_{DELAY} pin to adjust the delay from 1 ms to 300 ms.

The overtemperature and short circuit current-limiting provide additional protection for the LDO during system fault conditions.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

 † Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = (V_R + 0.5V)$ or 2.3V, whichever is greater, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 4.7 \,\mu\text{F}$ (X7R Ceramic), $T_A = +25^{\circ}\text{C}$. Boldface type applies for junction temperatures, T_J (Note 7) of -40°C to +125°C

C _{IN} - C _{OUT} - 4.7 pr (A7K Ceramic), 1 _A - +25 C. Boldrace type applies for junction temperatures, 1 _J (Note 7) or -40 C to +125 C							
Parameters	Sym	Min	Тур	Max	Units	Conditions	
Input Operating Voltage	V _{IN}	2.3		6.0	V	Note 1	
Input Quiescent Current	Iq	_	140	220	μA	$I_L = 0$ mA, $V_{IN} = V_R + 0.5V$, $V_{OUT} = 0.8V$ to 5.0V	
Input Quiescent Current for SHDN Mode	I _{SHDN}	_	0.1	3	μA	SHDN = GND	
Maximum Output Current	I _{OUT}	1	_	1	Α	V _{IN} = 2.3V to 6.0V (Note 1)	
Line Regulation	ΔV _{OUT} / (V _{OUT} x ΔV _{IN})	_	0.05	0.3	%/V	$(V_R + 0.5)V \le V_{IN} \le 6V$	
Load Regulation	ΔV _{OUT} /V _{OUT}	-1.5	±0.5	1.5	%	I _{OUT} = 1 mA to 1A, V _{IN} = (V _R + 0.6)V (Note 4)	
Output Short Circuit Current	I _{OUT_SC}	_	1.7	ı	Α	$V_{IN} = (V_R + 0.5)V,$ $R_{LOAD} < 0.1\Omega,$ Peak Current	
Adjust Pin Characteristics							
Adjust Pin Reference Voltage	V_{ADJ}	0.402	0.410	0.418	V	V_{IN} = 2.3V to V_{IN} = 6.0V, I_{OUT} = 1 mA	
Adjust Pin Leakage Current	I _{ADJ}	-10	±0.01	+10	nA	$V_{IN} = 6.0V, V_{ADJ} = 0V \text{ to } 6V$	
Adjust Temperature Coefficient	TCV _{OUT}	_	40	1	ppm/°C	Note 3	
Fixed-Output Characteristics							
Voltage Regulation	V _{OUT}	V _R - 2.5%	V _R ±0.5%	V _R + 2.5%	V	Note 2	
Dropout Characteristics							
Dropout Voltage	V _{IN} -V _{OUT}	_	220	500	mV	I _{OUT} = 1A, V _{IN(MIN)} = 2.3V (Note 5)	

- Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \ge 2.3 V$ and $V_{IN} \ge (V_R + 2.5\%) + V_{DROPOUT}$.
 - 2: V_R is the nominal regulator output voltage for the fixed cases. V_R = 1.2V, 1.8V, etc. V_R is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} * ((R_1/R_2)+1)$. Figure 4-1.
 - 3: TCV_{OUT} = (V_{OUT-HIGH} V_{OUT-LOW}) *10⁶ / (V_R * ΔTemperature). V_{OUT-HIGH} is the highest voltage measured over the temperature range. V_{OUT-LOW} is the lowest voltage measured over the temperature range.
 - 4: Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.
 - 5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + 0.5V$.
 - 6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 125°C can impact device reliability.
 - 7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = (V_R + 0.5V)$ or 2.3V, whichever is greater, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 4.7 \,\mu\text{F}$ (X7R Ceramic), $T_A = +25^{\circ}\text{C}$. **Boldface** type applies for junction temperatures, T_J (**Note 7**) of **-40°C to +125°C**

Parameters	Sym	Min	Тур	Max	Units	Conditions
Power Good Characteristics						
Input Voltage Operating Range	V _{PWRGD_VIN}	1.0	_	6.0	V	T _A = +25°C
for Valid PWRGD		1.2	_	6.0		$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$
						I _{SINK} = 100 μA
PWRGD Threshold Voltage	PWRGD_THF	88	92	96	%	V _{OUT} < 2.5V, Falling Edge
(Referenced to V _{OUT})		89	92	95	%	V _{OUT} > 2.5V, Falling Edge
	PWRGD_THR	89	94	98	%	V _{OUT} < 2.5V, Rising Edge
		90	93	96	%	V _{OUT} > 2.5V, Rising Edge
PWRGD Output Voltage Low	V _{PWRGD_L}	_	0.2	0.4	V	I _{PWRGD SINK} = 1.2 mA
PWRGD Leakage	P _{WRGD_LK}	_	0.1	_	μΑ	$V_{PWRGD} = V_{IN} = 6.0V$
PWRGD Time Delay	T _{PG}	_	200	_	μs	C _{DELAY} = OPEN
		10	30	55	ms	$C_{DELAY} = 0.01 \mu F$
		_	300	_	ms	$C_{DELAY} = 0.1 \mu F$
Detect Threshold to PWRGD Active Time Delay	T _{VDET-PWRGD}	1	170	_	μs	
Shutdown Input						
Logic-High Input	V _{SHDN-HIGH}	45			%V _{IN}	V _{IN} = 2.3V to 6.0V
Logic-Low Input	V _{SHDN-Low}			15	%V _{IN}	V _{IN} = 2.3V to 6.0V
SHDN Input Leakage Current	SHDN _{ILK}	-0.1	±0.001	+0.1	μA	$V_{IN} = 6V$, $\overline{SHDN} = V_{IN}$, $\overline{SHDN} = GND$
AC Performance						
Output Delay From SHDN	T _{OR}		100		μs	$\overline{\text{SHDN}}$ = GND to V _{IN} V _{OUT} = GND to 95% V _R
Output Noise	e _N	1	2.0		μV/√Hz	$\begin{split} I_{OUT} &= 200 \text{ mA, f} = 1 \text{ kHz,} \\ C_{OUT} &= 1 \mu\text{F (X7R Ceramic),} \\ V_{OUT} &= 2.5 \text{V} \end{split}$
Power Supply Ripple Rejection Ratio	PSRR	_	54	_	dB	$ f = 100 \text{ Hz}, C_{OUT} = 10 \mu\text{F}, \\ I_{OUT} = 100 \text{ mA}, \\ V_{INAC} = 30 \text{ mV pk-pk}, \\ C_{IN} = 0 \mu\text{F} $
Thermal Shutdown Temperature	T _{SD}	_	150	_	°C	I _{OUT} = 100 μA, V _{OUT} = 1.8V, V _{IN} = 2.8V
Thermal Shutdown Hysteresis	ΔT _{SD}	_	10	_	°C	I _{OUT} = 100 μA, V _{OUT} = 1.8V, V _{IN} = 2.8V

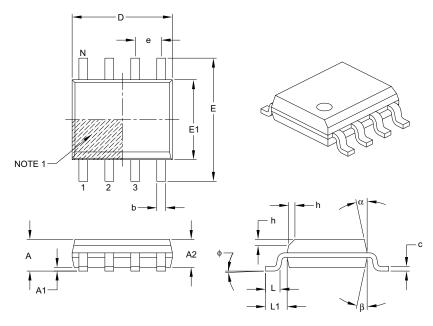
- Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \ge 2.3V$ and $V_{IN} \ge (V_R + 2.5\%) + V_{DROPOUT}$.
 - 2: V_R is the nominal regulator output voltage for the fixed cases. V_R = 1.2V, 1.8V, etc. V_R is the desired set point output voltage for the adjustable cases. V_R = V_{ADJ} * ((R_1/R_2)+1). Figure 4-1.
 - 3: $TCV_{OUT} = (V_{OUT-HIGH} V_{OUT-LOW}) *10^6 / (V_R * \Delta Temperature)$. $V_{OUT-HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT-LOW}$ is the lowest voltage measured over the temperature range.
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 - 7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

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TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all limits apply for V _{IN} = 2.3V to 6.0V.						
Parameters	Sym	Min	Тур	Max	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T _J	-40	_	+125	°C	Steady State
Maximum Junction Temperature	TJ	_	_	+150	°C	Transient
Storage Temperature Range	T _A	-65	_	+150	°C	
Thermal Package Resistances	•	•				
Thermal Resistance, 8LD 3x3 DFN	θ_{JA}	_	41	_	°C/W	4-Layer JC51-7 Standard Board with vias
Thermal Resistance, 8LD SOIC	θ_{JA}	_	150	_	°C/W	4-Layer JC51-7 Standard Board

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]



	Units	MILLIMETERS			
Di	mension Limits	MIN	NOM	MAX	
Number of Pins	N	8			
Pitch	е	1.27 BSC			
Overall Height	A	_	_	1.75	
Molded Package Thickness	A2	1.25	_	_	
Standoff §	A1	0.10	_	0.25	
Overall Width	E	6.00 BSC			
Molded Package Width	E1	3.90 BSC			
Overall Length	D	4.90 BSC			
Chamfer (optional)	h	0.25	_	0.50	
Foot Length	L	0.40	_	1.27	
Footprint	L1	1.04 REF			
Foot Angle	ф	0°	_	8°	
Lead Thickness	С	0.17	_	0.25	
Lead Width	b	0.31	_	0.51	
Mold Draft Angle Top	α	5°	_	15°	
Mold Draft Angle Bottom	β	5°	_	15°	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - $\label{eq:REF:Reference Dimension, usually without tolerance, for information purposes only. \\$

Microchip Technology Drawing C04-057B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. X Device Tape Ree	• · · · · · · · · · · · · · · · · · · ·	Examples: a) MCP1726-0802E/MF: 0.8V, 1A LDO, 8LD DFN Pkg. b) MCP1726-1202E/SN: 1.20V, 1A LDO, 8LD SOIC Pkg.
Device	MCP1726:1A, Low Quiescent Current LDO Regulator	c) MCP1726T-1802E/MF:Tape and Reel, 1.80V, 1A LDO, 8LD DFN Pkg.
Tape & Reel	T = Tape and Reel Blank = Tube	d) MCP1726-2502E/SN: 2.50V, 1A LDO, 8LD SOIC Pkg.
Standard Output	080 = 0.80V	e) MCP1726-3002E/MF: 3.00V, 1A LDO, 8LD DFN Pkg.
Voltage *	120 = 1.20V 180 = 1.80V	f) MCP1726T-3302E/MF:Tape and Reel, 3.30V, 1A LDO, 8LD DFN Pkg.
	250 = 2.50V 300 = 3.00V	g) MCP1726-5002E/SN: 5.00V, 1A LDO, 8LD SOIC Pkg.
	330 = 3.30V 500 = 5.00V ADJ = Adjustable Voltage Version	h) MCP1726-ADJE/MF: Adjustable, , 1A LDO, 8LD DFN Pkg.
	* Custom output voltages available upon request. Contact your local Microchip sales office for more information.	
Tolerance	2 = 2.0%	
Temperature Range	E = -40°C to +125°C	
Package *	SN = Plastic SOIC, (150 mil Body) 8-Lead MF = Plastic Dual Flat No Lead, 3x3 mm Body (DFN), 8-Lead	
	*Both packages are Lead Free.	