MCP6V01/2/3

300 µA, Auto-Zeroed Op Amps

Features

- High DC Precision:
  - V_{OS} Drift: ±50 nV/°C (maximum)
  - V_{OS}: ±2 µV (maximum)
  - A_{OL}: 130 dB (minimum)
  - PSRR: 130 dB (minimum)
  - CMRR: 130 dB (minimum)
  - E_{ni}: 2.5 μV_{P-P} (typical), f = 0.1 Hz to 10 Hz
  - E_{ni}: 0.79 µVp-p (typical), f = 0.01 Hz to 1 Hz
- Low Power and Supply Voltages:
  - I_Q: 300 µA/amplifier (typical)
  - Wide Supply Voltage Range: 1.8V to 5.5V
- Easy to Use:
  - Rail-to-Rail Input/Output
  - Gain Bandwidth Product: 1.3 MHz (typical)
  - Unity Gain Stable
  - Available in Single and Dual
  - Single with Chip Select ($\overline{CS}$): MCP6V03
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- Portable Instrumentation
- Sensor Conditioning
- Temperature Measurement
- DC Offset Correction
- Medical Instrumentation

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Related Parts

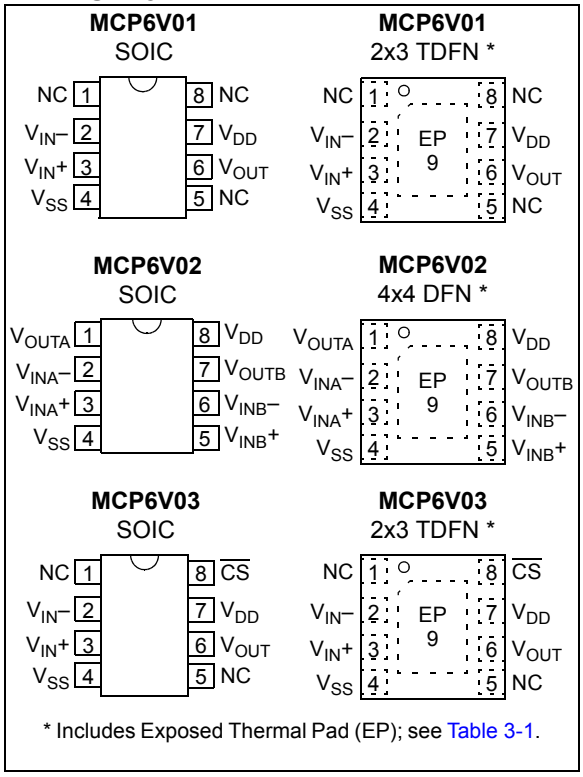
- MCP6V06/7/8: Non-spread clock, lower noise

Description

The Microchip Technology Inc. MCP6V01/2/3 family of operational amplifiers has input offset voltage correction for very low offset and offset drift. These devices have a wide gain bandwidth product (1.3 MHz, typical) and strongly reject switching noise. They are unity gain stable, have no 1/f noise, and have good PSRR and CMRR. These products operate with a single supply voltage as low as 1.8V, while drawing 300 µA/amplifier (typical) of quiescent current.

The Microchip Technology Inc. MCP6V01/2/3 op amps are offered in single (MCP6V01), single with Chip Select ($\overline{CS}$) (MCP6V03), and dual (MCP6V02). They are designed in an advanced CMOS process.

Package Types (top view)



* Includes Exposed Thermal Pad (EP); see Table 3-1.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.5V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN}+ and V_{IN}–) †† ... V_{SS} – 1.0V to V_{DD}+1.0V
All other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD}+0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....-65°C to +150°C
Max. Junction Temperature .....+150°C
ESD protection on all pins (HBM, MM) .....≥ 4 kV, 300V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.2.1 "Rail-to-Rail Inputs"**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-2.0	—	+2.0	µV	T_A = +25°C **(Note 1)**
Input Offset Voltage Drift with Temperature (linear Temp. Co.)	TC_1	-50	—	+50	nV/°C	T_A = -40 to +125°C **(Note 1)**
Input Offset Voltage Quadratic Temp. Co.	TC_2	—	±0.1	—	nV/°C^2	T_A = -40 to +125°C
Power Supply Rejection	PSRR	130	143	—	dB	**(Note 1)**
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1	—	pA	
Input Bias Current across Temperature	I_B	—	60	—	pA	T_A = +85°C
	I_B	—	600	5000	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	-30	—	pA	
Input Offset Current across Temperature	I_{OS}	—	-50	—	pA	T_A = +85°C
	I_{OS}	-1000	-75	1000	pA	T_A = +125°C
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode						
Common-Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.20	—	V_{DD} + 0.20	V	**(Note 2)**
Common-Mode Rejection	CMRR	130	142	—	dB	V_{DD} = 1.8V, V_{CM} = -0.2V to 2.0V (**Note 1, Note 2**)
	CMRR	140	152	—	dB	V_{DD} = 5.5V, V_{CM} = -0.2V to 5.7V (**Note 1, Note 2**)
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	130	145	—	dB	V_{DD} = 1.8V, V_{OUT} = 0.2V to 1.6V **(Note 1)**
	A_{OL}	140	156	—	dB	V_{DD} = 5.5V, V_{OUT} = 0.2V to 5.3V **(Note 1)**

Note 1: Set by design and characterization. Due to thermal junction and other effects in the production environment, these parts can only be screened in production (except TC_1; see **Appendix B: "Offset Related Test Screens"**).

2: Figure 2-18 shows how V_{CMR} changed across temperature for the first three production lots.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 15	mV	G = +2, 0.5V input overdrive
Output Short Circuit Current	I_{SC}	—	±7	—	mA	V_{DD} = 1.8V
	I_{SC}	—	±22	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per amplifier	I_Q	200	300	400	µA	I_O = 0
POR Trip Voltage	V_{POR}	1.15	—	1.65	V	

Note 1: Set by design and characterization. Due to thermal junction and other effects in the production environment, these parts can only be screened in production (except TC_1; see **Appendix B: "Offset Related Test Screens"**).

2: Figure 2-18 shows how V_{CMR} changed across temperature for the first three production lots.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Amplifier AC Response						
Gain Bandwidth Product	GBWP	—	1.3	—	MHz	
Slew Rate	SR	—	0.5	—	V/µs	
Phase Margin	PM	—	65	—	°	G = +1
Amplifier Noise Response						
Input Noise Voltage	E_{ni}	—	0.79	—	$µV_{P-P}$	f = 0.01 Hz to 1 Hz
	E_{ni}	—	2.5	—	$µV_{P-P}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	120	—	nV/√Hz	f < 2.5 kHz
	e_{ni}	—	45	—	nV/√Hz	f = 100 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	
Amplifier Distortion (Note 1)						
Intermodulation Distortion (AC)	IMD	—	<1	—	$µV_{PK}$	V_{CM} tone = 50 mV_{PK} at 1 kHz, G_N = 1, V_{DD} = 1.8V
	IMD	—	<1	—	$µV_{PK}$	V_{CM} tone = 50 mV_{PK} at 1 kHz, G_N = 1, V_{DD} = 5.5V
Amplifier Step Response						
Start Up Time	t_{STR}	—	500	—	µs	V_{OS} within 50 µV of its final value
Offset Correction Settling Time	t_{STL}	—	300	—	µs	G = +1, V_{IN} step of 2V, V_{OS} within 50 µV of its final value
Output Overdrive Recovery Time	t_{ODR}	—	100	—	µs	G = -100, ±0.5V input overdrive to V_{DD}/2, V_{IN} 50% point to V_{OUT} 90% point **(Note 2)**

Note 1: These parameters were characterized using the circuit in Figure 1-7. Figure 2-37 and Figure 2-38 show both an IMD tone at DC and a residual tone at1 kHz; all other IMD and clock tones are spread by the randomization circuitry.

2: t_{ODR} includes some uncertainty due to clock edge timing.

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TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 20 kΩ to V_L, C_L = 60 pF, and $\overline{CS}$ = GND (refer to Figure 1-5 and Figure 1-6).						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
$\overline{CS}$ Pull-Down Resistor (MCP6V03)						
$\overline{CS}$ Pull-Down Resistor	R_{PD}	3	5	—	MΩ	
$\overline{CS}$ Low Specifications (MCP6V03)						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.3V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5	—	pA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications (MCP6V03)						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.7V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	V_{DD}/R_{PD}	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, GND Current per amplifier	I_{SS}	—	-0.7	—	µA	$\overline{CS}$ = V_{DD}, V_{DD} = 1.8V
	I_{SS}	—	-2.3	—	µA	$\overline{CS}$ = V_{DD}, V_{DD} = 5.5V
Amplifier Output Leakage, $\overline{CS}$ High	I_{O_LEAK}	—	20	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Dynamic Specifications (MCP6V03)						
$\overline{CS}$ Low to Amplifier Output On Turn-on Time	t_{ON}	—	11	100	µs	$\overline{CS}$ Low = V_{SS}+0.3 V, G = +1 V/V, V_{OUT} = 0.9 V_{DD}/2
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	10	—	µs	$\overline{CS}$ High = V_{DD} – 0.3 V, G = +1 V/V, V_{OUT} = 0.1 V_{DD}/2
Internal Hysteresis	V_{HYST}	—	0.25	—	V	

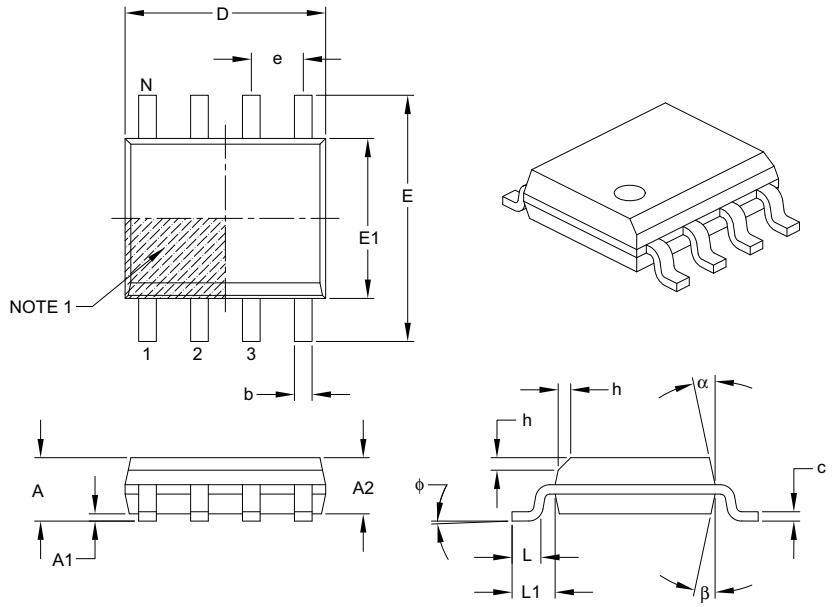
TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = +1.8V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-2x3 TDFN	θ_{JA}	—	41	—	°C/W	
Thermal Resistance, 8L-4x4 DFN	θ_{JA}	—	44	—	°C/W	**(Note 2)**
Thermal Resistance, 8L-SOIC	θ_{JA}	—	150	—	°C/W	

Note 1: Operation must not cause T_J to exceed Maximum Junction Temperature specification (150°C).

2: Measured on a standard JC51-7, four layer printed circuit board with ground plane and vias.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

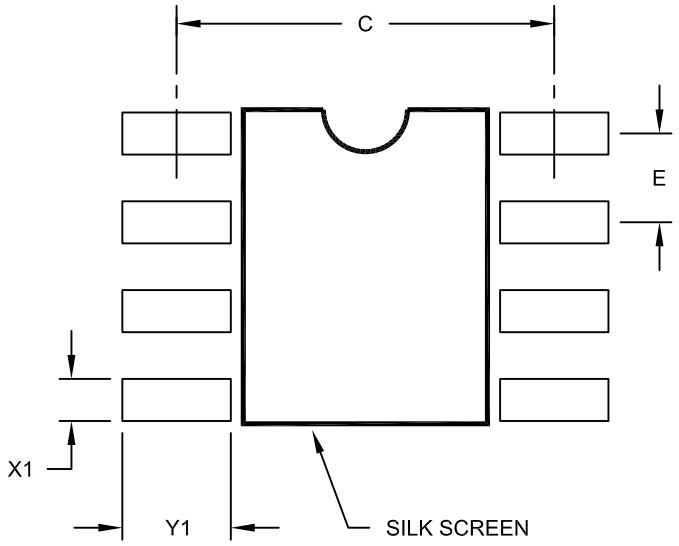
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–X	/XXX
Device	Temperature Range	Package

Device:	MCP6V01	Single Op Amp
	MCP6V01T	Single Op Amp (Tape and Reel for 2x3 TDFN andSOIC)
	MCP6V02	Dual Op Amp
	MCP6V02T	Dual Op Amp (Tape and Reel for 4×4 DFN and SOIC)
	MCP6V03	Single Op Amp with Chip Select
	MCP6V03T	Single Op Amp with Chip Select (Tape and Reel for SOIC)
Temperature Range:	E =	-40°C to +125°C
Package:	MD =	Plastic Dual Flat, No-Lead (4×4x0.9 mm), 8-lead (MCP6V02 only)
	MNY * =	Plastic Dual Flat No Lead (2x3x0.75 mm), 8-lead (MCP6V01, MCP6V03)
	SN =	Plastic SOIC (150mil Body), 8-lead

* Y = nickel palladium gold manufacturing designator. Only available on the TDFN package.

Examples:

a) MCP6V01T-E/SN: Extended temperature, 8LD SOIC package.

b) MCP6V01-E/MNY: Extended temperature, 8LD 2x3 TDFN package.

a) MCP6V02-E/MD: Extended temperature, 8LD 4x4 DFN package.

b) MCP6V02T-E/SN: Tape and Reel, Extended temperature, 8LD SOIC package.

a) MCP6V03-E/SN: Extended temperature, 8LD SOIC package.

b) MCP6V03-E/MNY: Extended temperature, 8LD 2x3 TDFN package.