MCP6S91/2/3

Single-Ended, Rail-to-Rail I/O, Low-Gain PGA

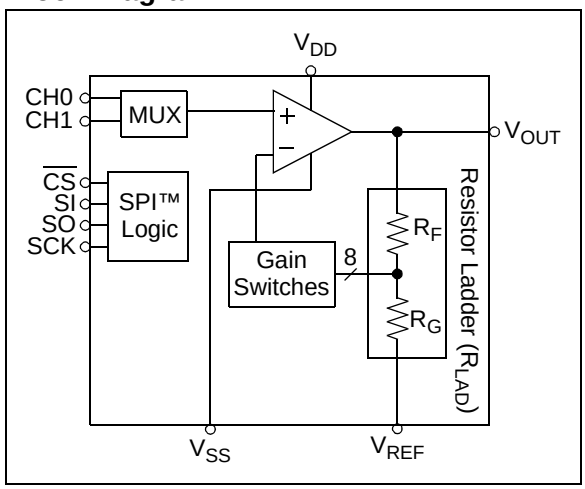
Features

- Multiplexed Inputs: 1 or 2 channels
- 8 Gain Selections:
  - +1, +2, +4, +5, +8, +10, +16 or +32 V/V
- Serial Peripheral Interface (SPI™)
- Rail-to-Rail Input and Output
- Low Gain Error: ±1% (max.)
- Offset Mismatch Between Channels: 0 µV
- High Bandwidth: 1 to 18 MHz (typ.)
- Low Noise: 10 nV/√Hz @ 10 kHz (typ.)
- Low Supply Current: 1.0 mA (typ.)
- Single Supply: 2.5V to 5.5V
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- A/D Converter Driver
- Multiplexed Analog Applications
- Data Acquisition
- Industrial Instrumentation
- Test Equipment
- Medical Instrumentation

Block Diagram

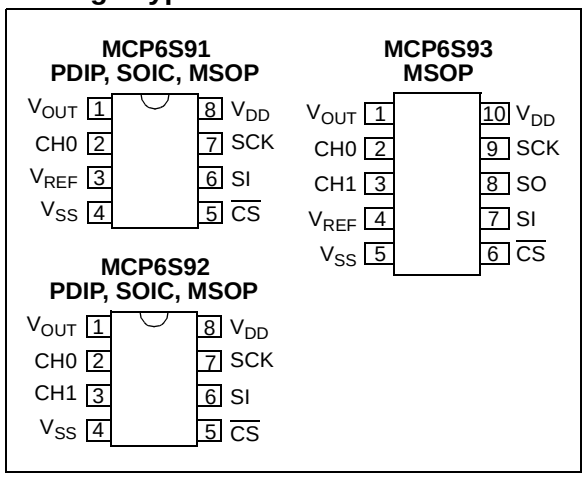


Description

The Microchip Technology Inc. MCP6S91/2/3 are analog Programmable Gain Amplifiers (PGAs). They can be configured for gains from +1 V/V to +32 V/V and the input multiplexer can select one of up to two channels through a SPI port. The serial interface can also put the PGA into shutdown to conserve power. These PGAs are optimized for high-speed, low offset voltage and single-supply operation with rail-to-rail input and output capability. These specifications support single-supply applications needing flexible performance or multiple inputs.

The one-channel MCP6S91 and the two-channel MCP6S92 are available in 8-pin PDIP, SOIC and MSOP packages. The two-channel MCP6S93 is available in a 10-pin MSOP package. All parts are fully specified from -40°C to +125°C.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
All inputs and outputs..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....continuous
Current at Input Pin .....±2 mA
Current at Output and Supply Pins..... ±30 mA
Storage temperature .....-65°C to +150°C
Junction temperature .....+150°C
ESD protection on all pins (HBM; MM) ..... ≥ 4 kV; 200V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{OUT}	Analog Output
CH0, CH1	Analog Inputs
V_{REF}	External Reference Pin
V_{SS}	Negative Power Supply
$\overline{CS}$	SPI Chip Select
SI	SPI Serial Data Input
SO	SPI Serial Data Output
SCK	SPI Clock Input
V_{DD}	Positive Power Supply

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to $V_{DD}/2$, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters		Sym	Min	Typ	Max	Units	Conditions
Amplifier Inputs (CH0, CH1)							
Input Offset Voltage		V_{OS}	-4	—	+4	mV	G = +1
Input Offset Voltage Mismatch		ΔV_{OS}	—	0	—	µV	Between inputs (CH0, CH1)
Input Offset Voltage Drift		$\Delta V_{OS}/\Delta T_A$	—	±1.8	—	µV/°C	T_A = -40°C to +125°C
Power Supply Rejection Ratio		PSRR	70	90	—	dB	G = +1 **(Note 1)**
Input Bias Current		I_B	—	±1	—	pA	CHx = $V_{DD}/2$
Input Bias Current at Temperature		I_B	—	30	—	pA	CHx = $V_{DD}/2$, T_A = +85°C
		I_B	—	600	—	pA	CHx = $V_{DD}/2$, T_A = +125°C
Input Impedance		Z_{IN}	—	10^{13}‖7	—	Ω‖pF	
Input Voltage Range		V_{IVR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	**(Note 2)**
Reference Input (V_{REF})							
Input Impedance		Z_{IN_REF}	—	(5/G)‖6	—	kΩ‖pF	
Voltage Range		V_{IVR_REF}	V_{SS}	—	V_{DD}	V	**(Note 2)**
Amplifier Gain							
Nominal Gains		G	—	1 to 32	—	V/V	+1, +2, +4, +5, +8, +10, +16 or +32
DC Gain Error	G = +1	g_E	-0.2	—	+0.2	%	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V
	G ≥ +2	g_E	-1.0	—	+1.0	%	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V
DC Gain Drift	G = +1	$\Delta G/\Delta T_A$	—	±0.0002	—	%/°C	T_A = -40°C to +125°C
	G ≥ +2	$\Delta G/\Delta T_A$	—	±0.0004	—	%/°C	T_A = -40°C to +125°C

Note 1: R_{LAD} (R_F+R_G in Figure 4-1) connects V_{REF}, V_{OUT} and the inverting input of the internal amplifier. The MCP6S92 has V_{REF} tied internally to V_{SS}, so V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. It is recommended that the MCP6S92's V_{SS} pin be tied directly to ground to avoid noise problems.

2: The MCP6S92's V_{IVR} and V_{IVR_REF} are not tested in production; they are set by design and characterization.

3: I_Q includes current in R_{LAD} (typically 60 µA at V_{OUT} = 0.3V). Both I_Q and I_{Q_SHDN} exclude digital switching currents.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to $V_{DD}/2$, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Ladder Resistance						
Ladder Resistance	R_{LAD}	3.4	4.9	6.4	kΩ	**(Note 1)**
Ladder Resistance across Temperature	$\Delta R_{LAD}/\Delta T_A$	—	+0.028	—	%/°C	T_A = -40°C to +125°C **(Note 1)**
Amplifier Output						
DC Output Non-linearity G = +1	V_{ONL}	—	±0.18	—	% of FSR	$V_{OUT} \approx$ 0.3V to V_{DD} – 0.3V, V_{DD} = 5.0V
G ≥ +2	V_{ONL}	—	±0.050	—	% of FSR	$V_{OUT} \approx$ 0.3V to V_{DD} – 0.3V, V_{DD} = 5.0V
Maximum Output Voltage Swing	V_{OH_ANA}, V_{OL_ANA}	V_{SS} + 20	—	V_{DD} – 100	mV	G ≥ +2; 0.5V output overdrive
		V_{SS} + 60	—	V_{DD} – 60		G ≥ +2; 0.5V output overdrive, $V_{REF} = V_{DD}/2$
Short Circuit Current	I_{SC}	—	±25	—	mA	
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Minimum Valid Supply Voltage	V_{DD_VAL}	—	0.4	2.0	V	Register data still valid
Quiescent Current	I_Q	0.4	1.0	1.6	mA	I_O = 0 **(Note 3)**
Quiescent Current, Shutdown Mode	I_{Q_SHDN}	—	30	—	pA	I_O = 0 **(Note 3)**

Note 1: R_{LAD} (R_F+R_G in Figure 4-1) connects V_{REF}, V_{OUT} and the inverting input of the internal amplifier. The MCP6S92 has V_{REF} tied internally to V_{SS}, so V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. It is recommended that the MCP6S92's V_{SS} pin be tied directly to ground to avoid noise problems.

2: The MCP6S92's V_{IVR} and V_{IVR_REF} are not tested in production; they are set by design and characterization.

3: I_Q includes current in R_{LAD} (typically 60 µA at V_{OUT} = 0.3V). Both I_Q and I_{Q_SHDN} exclude digital switching currents.

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to V_{DD}/2, C_L = 60 pF, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Frequency Response						
-3 dB Bandwidth	BW	—	1 to 18	—	MHz	All gains; V_{OUT} < 100 mV_{P-P} **(Note 1)**
Gain Peaking	GPK	—	0	—	dB	All gains; V_{OUT} < 100 mV_{P-P}
Total Harmonic Distortion plus Noise						
f = 20 kHz, G = +1 V/V	THD+N	—	0.0011	—	%	V_{OUT} = 1.5V ± 1.0 V_{PK}, V_{DD} = 5.0V, BW = 80 kHz, R_L = 10 kΩ to 1.5V
f = 20 kHz, G = +1 V/V	THD+N	—	0.0089	—	%	V_{OUT} = 2.5V ± 1.0 V_{PK}, V_{DD} = 5.0V, BW = 80 kHz
f = 20 kHz, G = +4 V/V	THD+N	—	0.0045	—	%	V_{OUT} = 2.5V ± 1.0 V_{PK}, V_{DD} = 5.0V, BW = 80 kHz
f = 20 kHz, G = +16 V/V	THD+N	—	0.028	—	%	V_{OUT} = 2.5V ± 1.0 V_{PK}, V_{DD} = 5.0V, BW = 80 kHz
Step Response						
Slew Rate	SR	—	4.0	—	V/µs	G = 1, 2
		—	11	—	V/µs	G = 4, 5, 8, 10
		—	22	—	V/µs	G = 16, 32
Noise						
Input Noise Voltage	E_{ni}	—	4.5	—	μV_{P-P}	f = 0.1 Hz to 10 Hz **(Note 2)**
		—	30	—		f = 0.1 Hz to 200 kHz **(Note 2)**
Input Noise Voltage Density	e_{ni}	—	10	—	nV/√Hz	f = 10 kHz **(Note 2)**
Input Noise Current Density	i_{ni}	—	4	—	fA/√Hz	f = 10 kHz

Note 1: See Table 4-1 for a list of typical numbers and Figure 2-25 for the frequency response versus gain.

2: E_{ni} and e_{ni} include ladder resistance noise. See Figure 2-12 for e_{ni} versus G data.

DIGITAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = 25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 = 0.3V, R_L = 10 kΩ to V_{DD}/2, C_L = 60 pF, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
SPI Inputs ($\overline{CS}$, SI, SCK)						
Logic Threshold, Low	V_{IL}	0	—	0.3V_{DD}	V	
Input Leakage Current	I_{IL}	-1.0	—	+1.0	µA	
Logic Threshold, High	V_{IH}	0.7 V_{DD}	—	V_{DD}	V	
Amplifier Output Leakage Current	—	-1.0	—	1.0	µA	In Shutdown mode
SPI Output (SO, for MCP6S93)						
Logic Threshold, Low	V_{OL_DIG}	V_{SS}	—	V_{SS}+0.4	V	I_{OL} = 2.1 mA, V_{DD} = 5V
Logic Threshold, High	V_{OH_DIG}	V_{DD} – 0.5	—	V_{DD}	V	I_{OH} = -400 µA
SPI Timing						
Pin Capacitance	C_{PIN}	—	10	—	pF	All digital I/O pins
Input Rise/Fall Times ($\overline{CS}$, SI, SCK)	t_{RFI}	—	—	2	µs	**(Note 1)**
Output Rise/Fall Times (SO)	t_{RFO}	—	5	—	ns	**MCP6S93**
$\overline{CS}$ High Time	t_{CSH}	40	—	—	ns	
SCK Edge to $\overline{CS}$ Fall Setup Time	t_{CS0}	10	—	—	ns	SCK edge when $\overline{CS}$ is high
$\overline{CS}$ Fall to First SCK Edge Setup Time	t_{CSSC}	40	—	—	ns	
SCK Frequency	f_{SCK}	—	—	10	MHz	V_{DD} = 5V **(Note 2)**
SCK High Time	t_{HI}	40	—	—	ns	
SCK Low Time	t_{LO}	40	—	—	ns	
SCK Last Edge to $\overline{CS}$ Rise Setup Time	t_{SCCS}	30	—	—	ns	
$\overline{CS}$ Rise to SCK Edge Setup Time	t_{CS1}	100	—	—	ns	SCK edge when $\overline{CS}$ is high
SI Setup Time	t_{SU}	40	—	—	ns	
SI Hold Time	t_{HD}	10	—	—	ns	
SCK to SO Valid Propagation Delay	t_{DO}	—	—	80	ns	**MCP6S93**
$\overline{CS}$ Rise to SO Forced to Zero	t_{SOZ}	—	—	80	ns	**MCP6S93**
Channel and Gain Select Timing						
Channel Select Time	t_{CH}	—	1.5	—	µs	CHx = 0.6V, CHy = 0.3V, G = 1, CHx to CHy select, $\overline{CS}$ = 0.7 V_{DD} to V_{OUT} 90% point
Gain Select Time	t_G	—	1	—	µs	CHx = CHy = 0.3V, G = 5 to G = 1 select, $\overline{CS}$ = 0.7 V_{DD} to V_{OUT} 90% point
Shutdown Mode Timing						
Out of Shutdown mode ($\overline{CS}$ goes high) to Amplifier Output Turn-on Time	t_{ON}	—	3.5	10	µs	$\overline{CS}$ = 0.7 V_{DD} to V_{OUT} 90% point
Into Shutdown mode ($\overline{CS}$ goes high) to Amplifier Output High-Z Turn-off Time	t_{OFF}	—	1.5	—	µs	$\overline{CS}$ = 0.7 V_{DD} to V_{OUT} 90% point

Note 1: Not tested in production. Set by design and characterization.

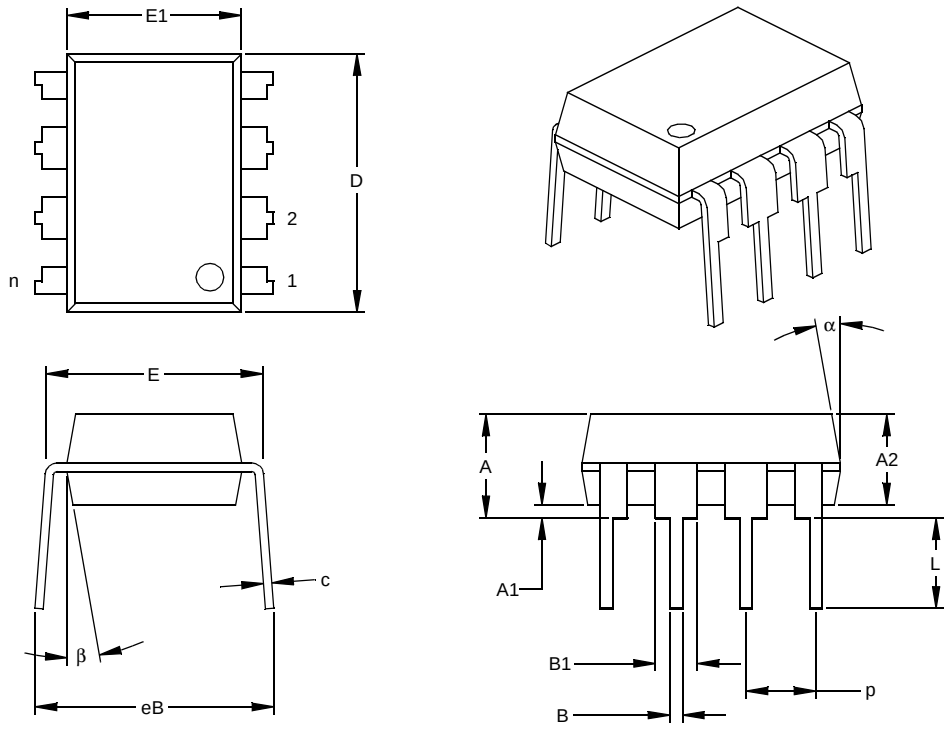
2: When using the device in the daisy-chain configuration, maximum clock frequency is determined by a combination of propagation delay time ($t_{DO} \leq$ 80 ns), data input set-up time ($t_{SU} \geq$ 40 ns), SCK high time ($t_{HI} \geq$ 40 ns) and SCK rise and fall times of 5 ns. Maximum f_{SCK} is therefore ≈ 5.8 MHz.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 10L-MSOP	θ_{JA}	—	143	—	°C/W	

Note 1: Operation in this range must not cause T_J to exceed Maximum Junction Temperature (+150°C).

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP6S91:	One-channel PGA
	MCP6S91T:	One-channel PGA (Tape and Reel for SOIC and MSOP-8)
	MCP6S92:	Two-channel PGA
	MCP6S92T:	Two-channel PGA (Tape and Reel for SOIC and MSOP-8)
	MCP6S93:	Two-channel PGA
	MCP6S93T:	Two-channel PGA (Tape and Reel for MSOP-10)
Temperature Range:	E =	-40°C to +125°C
Package:	MS =	Plastic Micro Small Outline (MSOP), 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	UN =	Plastic Micro Small Outline (MSOP), 10-lead

Examples:

a)	MCP6S91-E/P:	One-channel PGA, PDIP package.
b)	MCP6S91-E/SN:	One-channel PGA, SOIC package.
c)	MCP6S91-E/MS:	One-channel PGA, MSOP package.
a)	MCP6S92-E/MS:	Two-channel PGA, MSOP-8 package.
b)	MCP6S92T-E/MS:	Tape and Reel, Two-channel PGA, MSOP-8 package.
a)	MCP6S93-E/UN:	Two-channel PGA, MSOP-10 package.
b)	MCP6S93T-E/UN:	Tape and Reel, Two-channel PGA, MSOP-10 package.