



# MICROCHIP 24AA65/24LC65/24C65

## 64K I<sup>2</sup>C™ Smart Serial™ EEPROM

### Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
24AA65	1.8-6.0V	64 Bytes	C	P, SM
24LC65	2.5-6.0V	64 Bytes	C, I	P, SM
24C65	4.5-6.0V	64 Bytes	C, I, E	P, SM

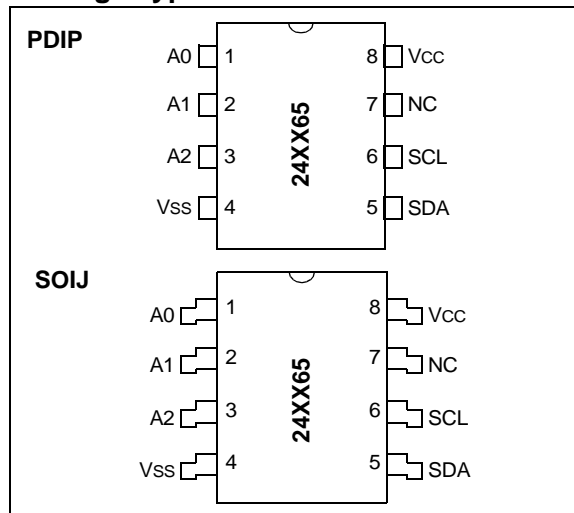
### Features:

- Voltage Operating Range: 1.8V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150  $\mu$ A at 6.0V
  - Standby current 1  $\mu$ A, typical
- Industry Standard Two-Wire Bus Protocol I<sup>2</sup>C™ Compatible
- 8-Byte Page, or Byte modes Available
- 2 ms Typical Write Cycle Time, Byte or Page
- 64-Byte Input Cache for Fast Write Loads
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory
- Including 100 kHz ( $1.8V \leq V_{cc} < 4.5V$ ) and 400 kHz ( $4.5V \leq V_{cc} \leq 6.0V$ ) Compatibility
- Programmable Block Security Options
- Programmable Endurance Options
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- Self-Timed Erase and Write Cycles
- Power-on/off Data Protection Circuitry
- Endurance:
  - 10,000,000 E/W cycles for a High Endurance Block
  - 1,000,000 E/W cycles for a Standard Endurance Block
- Electrostatic Discharge Protection > 4000V
- Data Retention > 200 years
- 8-pin PDIP/SOIJ Packages
- Temperature Ranges
  - Industrial (I) -40°C to +85°C
  - Automotive (E) -40°C to +125°C
- Pb-Free and RoHS Compliant

### Description:

The Microchip Technology Inc. 24AA65/24LC65/24C65 (24XX65)\* is a "smart" 8K x 8 Serial Electrically Erasable PROM. This device has been developed for advanced, low-power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24XX65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 1,000,000 erase/write (E/W) cycles ensured. The 24XX65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional address lines allow the connection of up to eight 24XX65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power nonvolatile code and data applications. The 24XX65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIJ package.

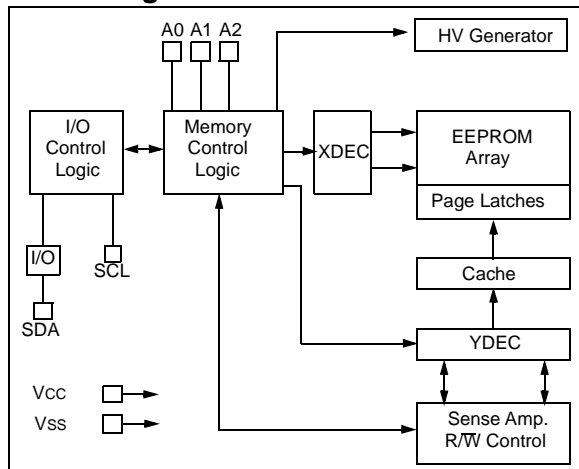
### Package Types



\*24XX65 is used in this document as a generic part number for the 24AA65/24LC65/24C65 devices.

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## Block Diagram



## Pin Function Table

Name	Function
A0, A1, A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data/I/O
SCL	Serial Clock
Vcc	+1.8V to 6.0V Power Supply
NC	<b>No Internal Connection</b>

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings<sup>(†)</sup>

V <sub>CC</sub> .....	7.0V
All inputs and outputs w.r.t. V <sub>SS</sub> .....	-0.6V to V <sub>CC</sub> +1.0V
Storage temperature .....	-65°C to +150°C
Ambient temperature with power applied.....	-40°C to +125°C
ESD protection on all pins .....	≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

DC CHARACTERISTICS		V <sub>CC</sub> = +1.8V to +6.0V			
		Commercial (C): T <sub>A</sub> = 0°C to +70°C			
		Industrial (I): T <sub>A</sub> = -40°C to +85°C			
		Automotive (E): T <sub>A</sub> = -40°C to +125°C			
Parameter	Sym	Min	Max	Units	Conditions
A0, A1, A2, SCL and SDA pins:					
High-level input voltage	V <sub>IH</sub>	.7 V <sub>CC</sub>	—	V	<b>(Note 1)</b> I <sub>OL</sub> = 3.0 mA
Low-level input voltage	V <sub>IL</sub>	—	.3 V <sub>CC</sub>	V	
Hysteresis of Schmitt Trigger inputs	V <sub>HYS</sub>	.05 V <sub>CC</sub>	—	V	
Low-level output voltage	V <sub>OL</sub>	—	.40	V	
Input leakage current	I <sub>LI</sub>	—	±1	μA	V <sub>IN</sub> = .1V to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	±1	μA	V <sub>OUT</sub> = .1V to V <sub>CC</sub>
Pin capacitance (all inputs/outputs)	C <sub>IN</sub> , C <sub>OUT</sub>	—	10	pF	V <sub>CC</sub> = 5.0V <b>(Note 1)</b> T <sub>A</sub> = 25°C, F <sub>CLK</sub> = 1 MHz
Operating current	I <sub>CC</sub> Write	—	3	mA	V <sub>CC</sub> = 6.0V, SCL = 400 kHz
	I <sub>CC</sub> Read	—	150	μA	V <sub>CC</sub> = 6.0V, SCL = 400 kHz
Standby current	I <sub>CCS</sub>	—	5	μA	V <sub>CC</sub> = 5.0V, SCL = SDA = V <sub>CC</sub> A0, A1, A2 = V <sub>SS</sub>

**Note 1:** This parameter is periodically sampled and not 100% tested.

**FIGURE 1-1: BUS TIMING START/STOP**



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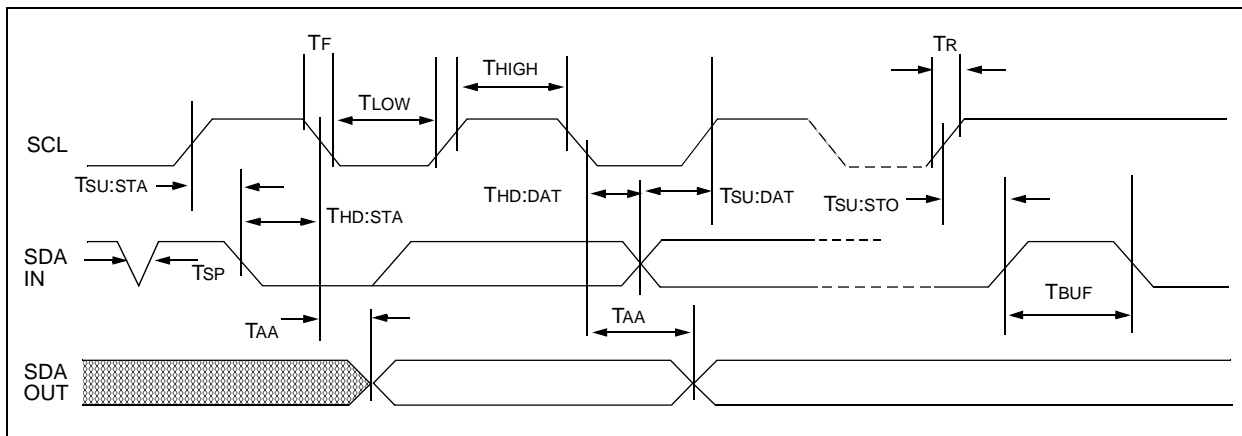
**TABLE 1-2: AC CHARACTERISTICS**

Parameter	Symbol	V <sub>CC</sub> = 1.8V-6.0V STD. Mode		V <sub>CC</sub> = 4.5-6.0V FAST Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	<b>(Note 1)</b>
SDA and SCL fall time	TF	—	300	—	300	ns	<b>(Note 1)</b>
Start condition setup time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
Start condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated Start condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
Stop condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	<b>(Note 2)</b>
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 Cb	250	ns	<b>(Note 1)</b> , C <sub>B</sub> ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	50	—	50	—	ns	<b>(Note 3)</b>
Write cycle time	TWR	—	5	—	5	ms/page	<b>(Note 4)</b>
Endurance							
High Endurance Block		10M	—	10M	—	cycles	25°C, <b>(Note 5)</b>
Rest of Array		1M	—	1M	—		

**Note 1:** Not 100 percent tested. C<sub>B</sub> = total capacitance of one bus line in pF.

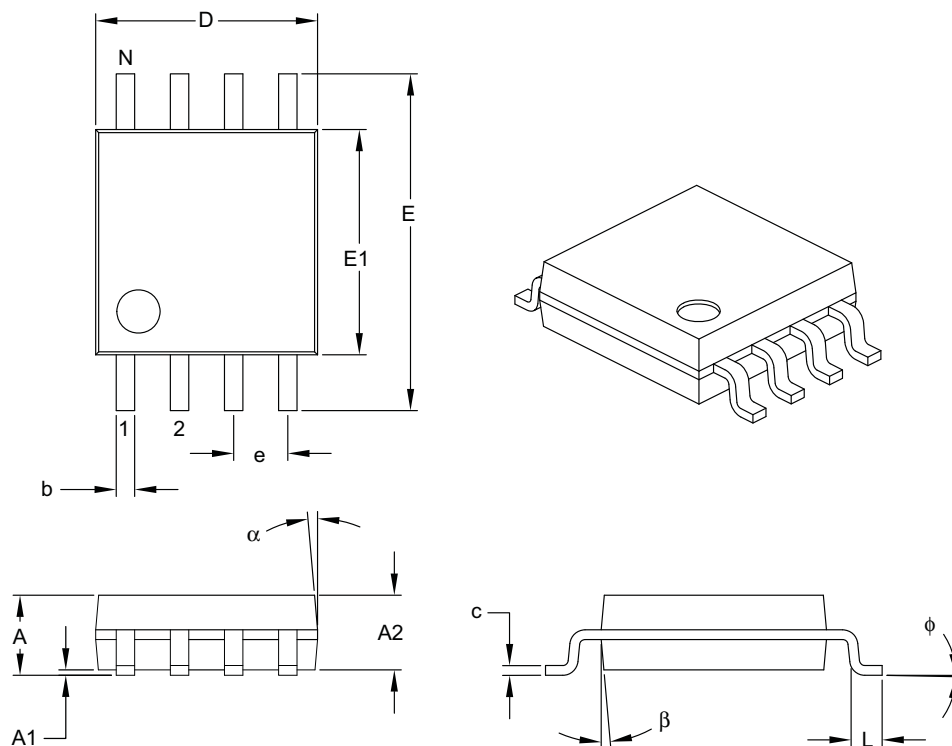
- 2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
- 3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.
- 4:** The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.
- 5:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model

**FIGURE 1-2: BUS TIMING DATA**



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## 8-Lead Plastic Small Outline (SM) – Medium, 5.28 mm Body [SOIJ]



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	1.77	–	2.03
Molded Package Thickness	A2	1.75	–	1.98
Standoff §	A1	0.05	–	0.25
Overall Width	E	7.62	–	8.26
Molded Package Width	E1	5.11	–	5.38
Overall Length	D	5.13	–	5.33
Foot Length	L	0.51	–	0.76
Foot Angle	$\phi$	0°	–	8°
Lead Thickness	c	0.15	–	0.25
Lead Width	b	0.36	–	0.51
Mold Draft Angle Top	$\alpha$	–	–	15°
Mold Draft Angle Bottom	$\beta$	–	–	15°

### Notes:

1. SOIJ, JEITA/EIAJ Standard, formerly called SOIC.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

Microchip Technology Drawing C04-056B

