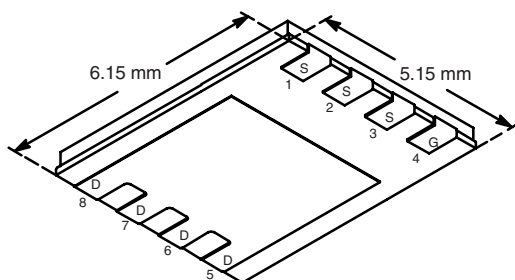


## N-Channel 40-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
40	0.0066 at $V_{GS} = 10$ V	40	16.1 nC
	0.008 at $V_{GS} = 4.5$ V	40	

PowerPAK® SO-8



Bottom View

Ordering Information: SiR422DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

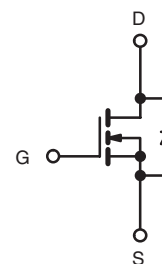
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 %  $R_g$  Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- POL
- Synchronous Rectification



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	40 <sup>a</sup>	A
		40 <sup>a</sup>	
		20.5 <sup>b, c</sup>	
		16.4 <sup>b, c</sup>	
Pulsed Drain Current	$I_{DM}$	70	
Avalanche Current	$I_{AS}$	30	
Avalanche Energy	$E_{AS}$	45	mJ
Continuous Source-Drain Diode Current	$I_S$	40 <sup>a</sup>	A
		4.1 <sup>b, c</sup>	
Maximum Power Dissipation	$P_D$	34.7	W
		22.2	
		5 <sup>b, c</sup>	
		3.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$R_{thJA}$	20	25	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	3.1	3.6	

Notes:

- Based on  $T_C = 25$  °C. Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$  s.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 70 °C/W.

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V	
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		46		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 5.8			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.2		2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μA	
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	50			A	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0054	0.0066	Ω	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A		0.0065	0.008		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		70		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1785		pF	
Output Capacitance	C <sub>oss</sub>			264			
Reverse Transfer Capacitance	C <sub>rss</sub>			120			
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		32	48	nC	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		16.1	25		
Gate-Drain Charge	Q <sub>gd</sub>			4.5			
Gate Resistance	R <sub>g</sub>			5.6			
Turn-On Delay Time	t <sub>d(on)</sub>	f = 1 MHz	0.2	0.8	1.6	Ω	
Rise Time	t <sub>r</sub>		V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		19	35	ns
Turn-Off Delay Time	t <sub>d(off)</sub>				84	145	
Fall Time	t <sub>f</sub>				28	55	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω			11	22	
Turn-On Delay Time	t <sub>d(on)</sub>			9	18		
Rise Time	t <sub>r</sub>			10	20		
Turn-Off Delay Time	t <sub>d(off)</sub>			20	40		
Fall Time	t <sub>f</sub>			8	16		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			40	A	
Pulse Diode Forward Current	I <sub>SM</sub>				70		
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 4.0 A, V <sub>GS</sub> = 0 V		0.76	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		25	40	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			14	25	nC	
Reverse Recovery Fall Time	t <sub>a</sub>			13		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			9			

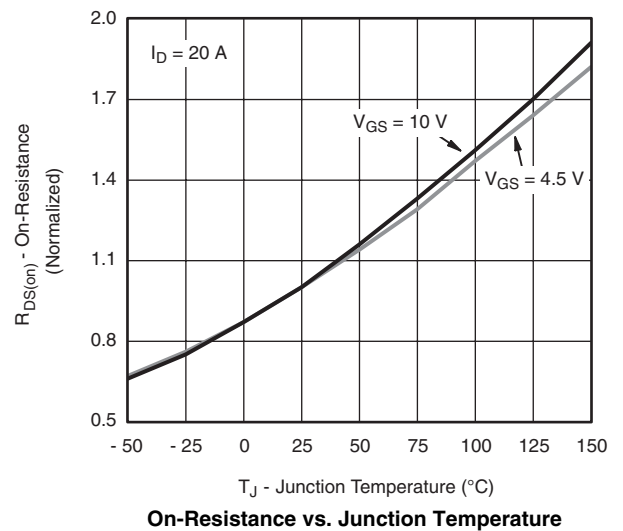
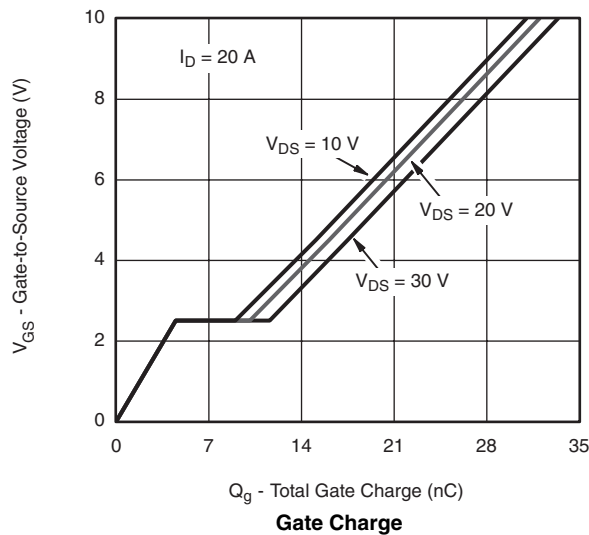
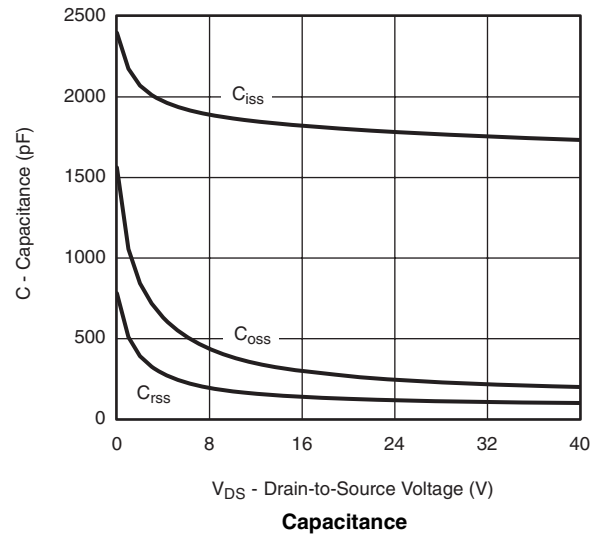
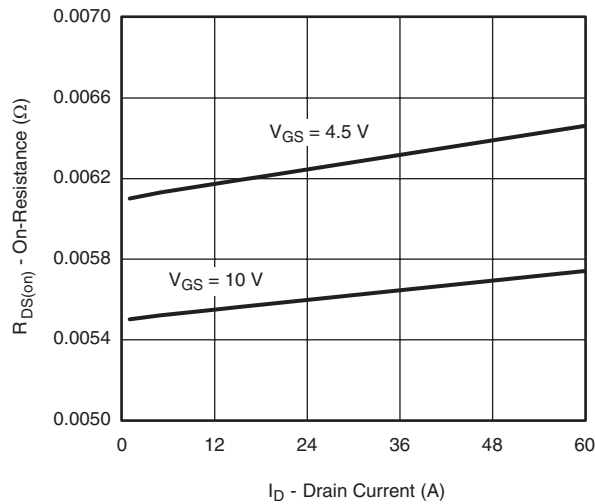
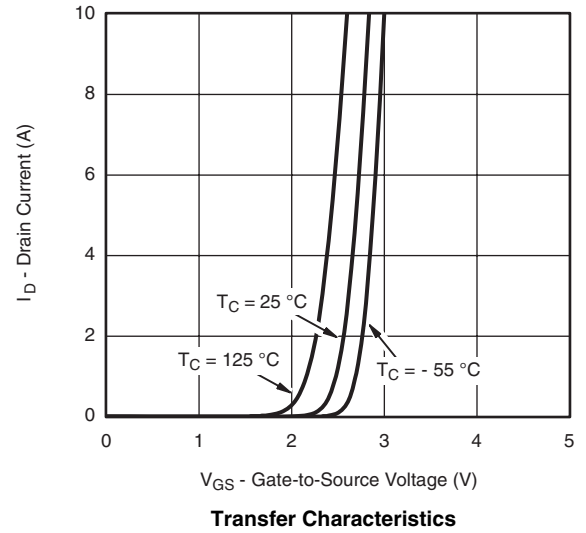
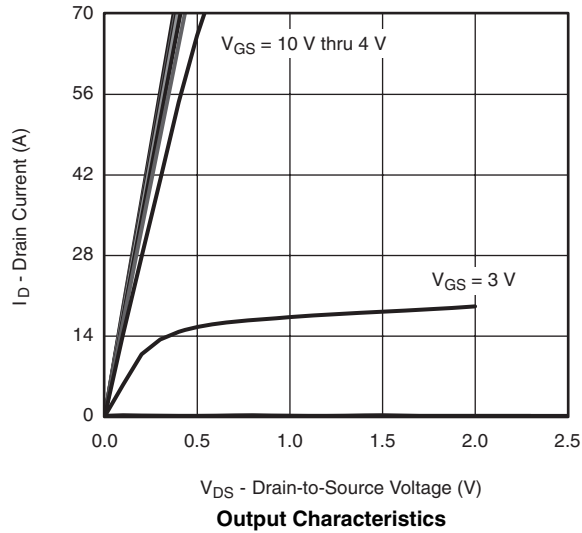
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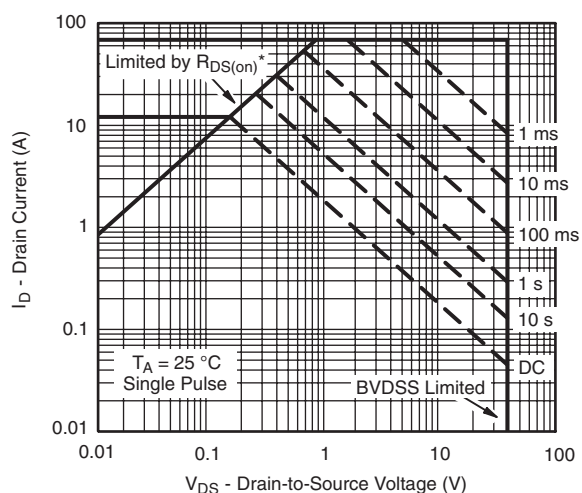
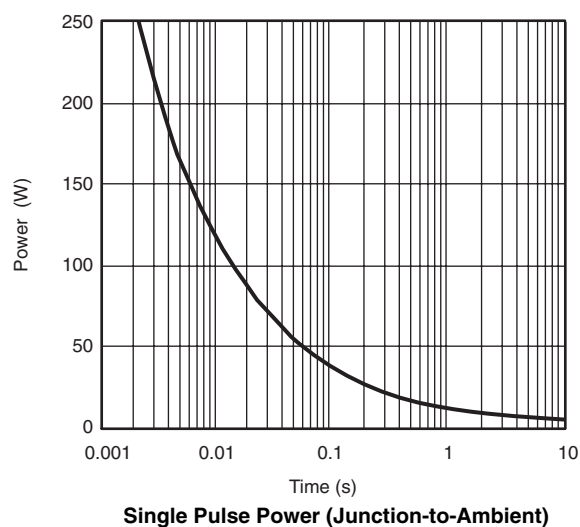
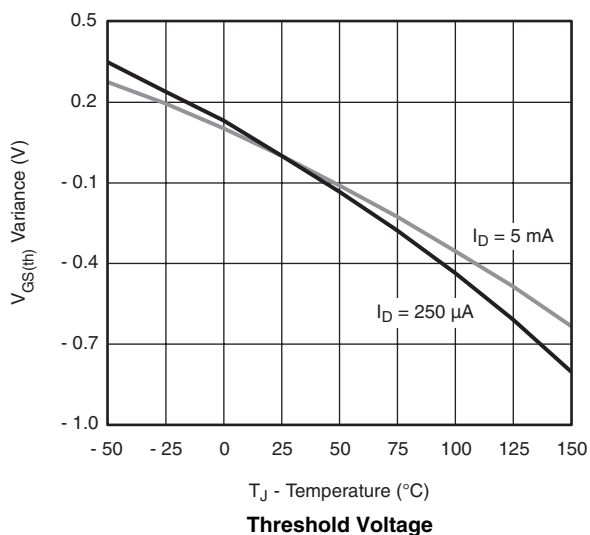
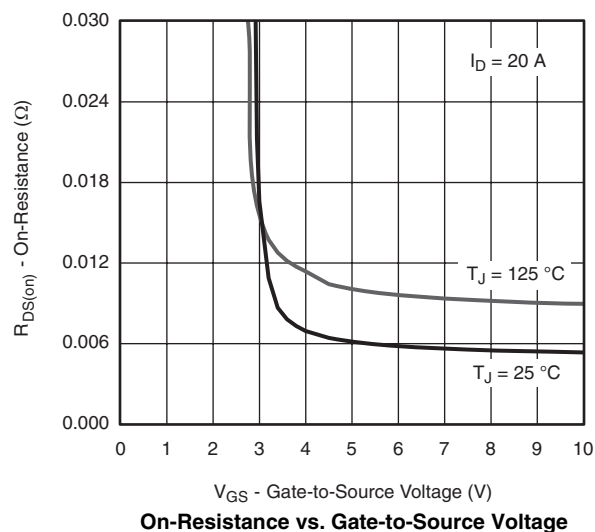
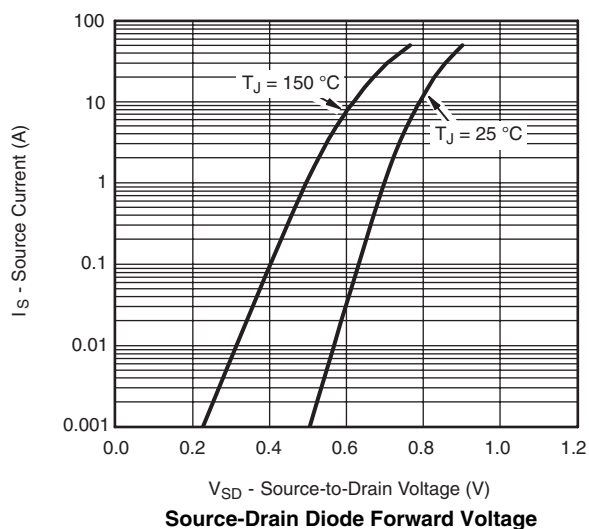
a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

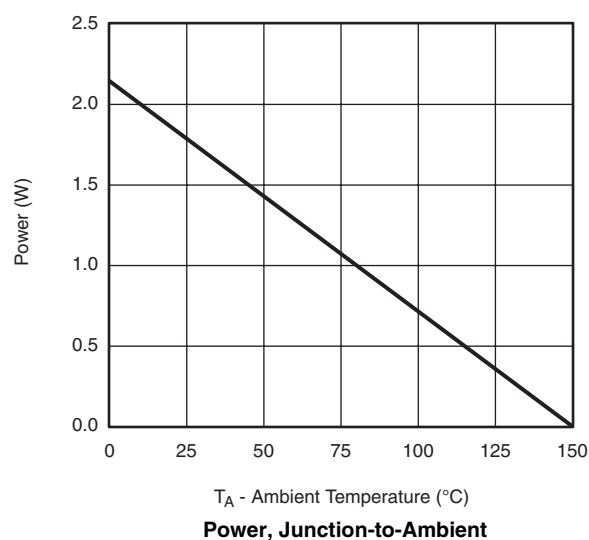
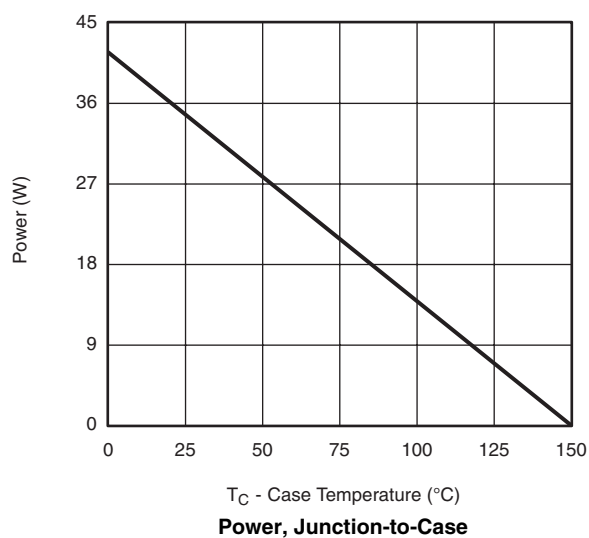
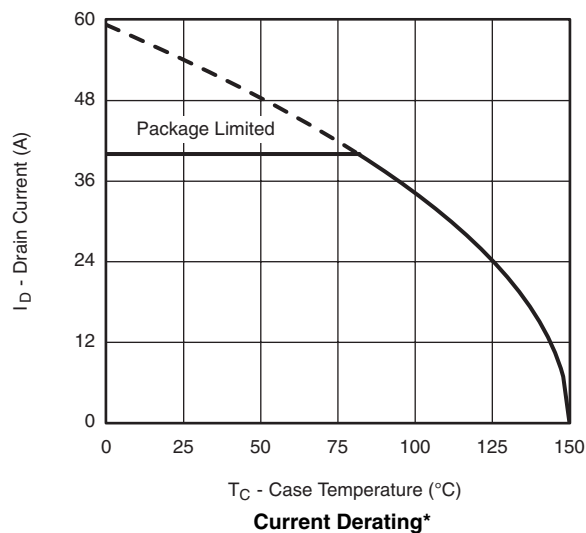


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

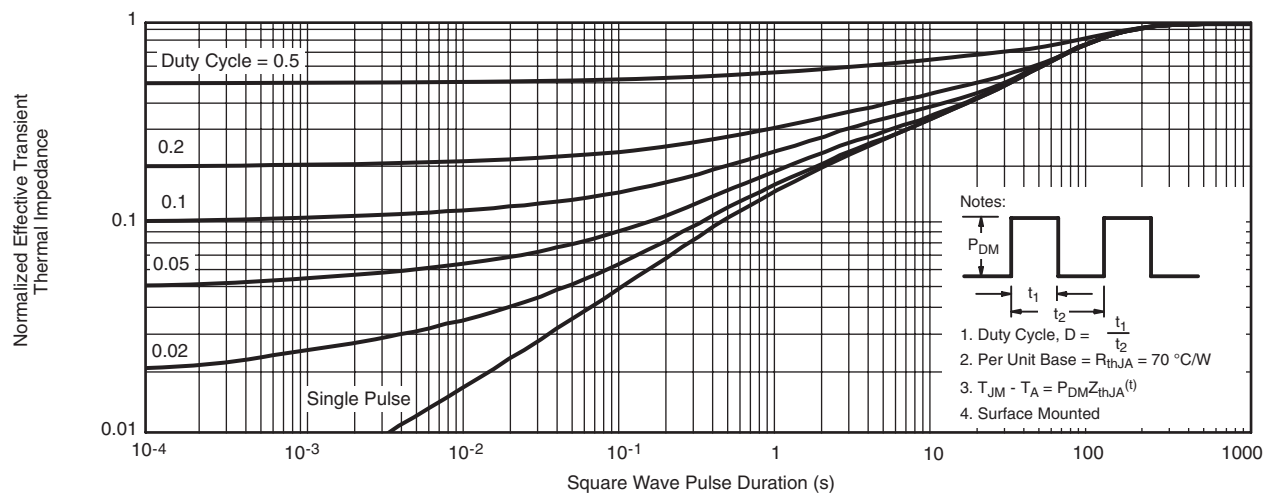
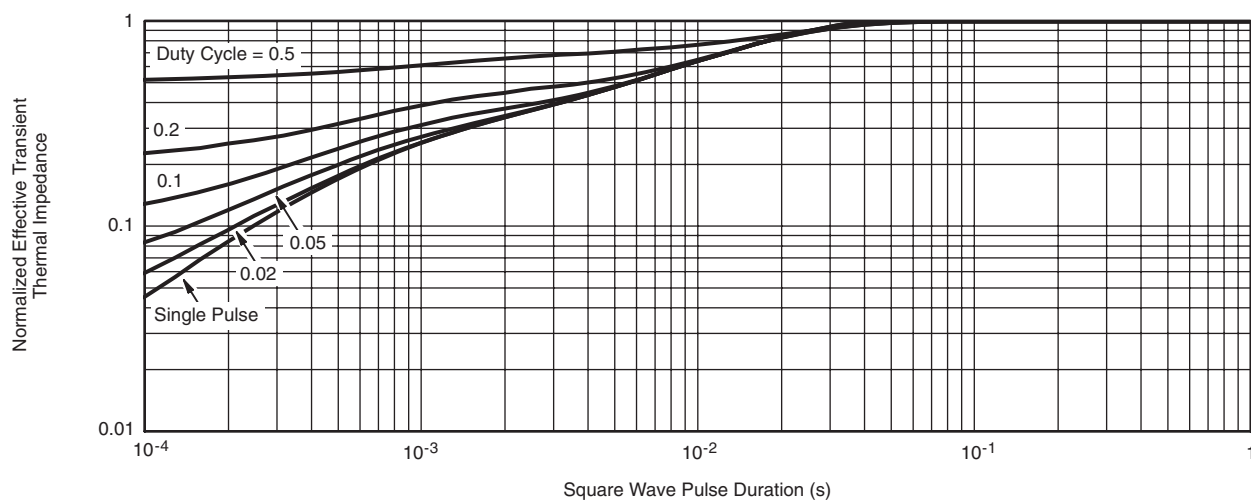
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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