Precision Quad SPDT Analog Switch

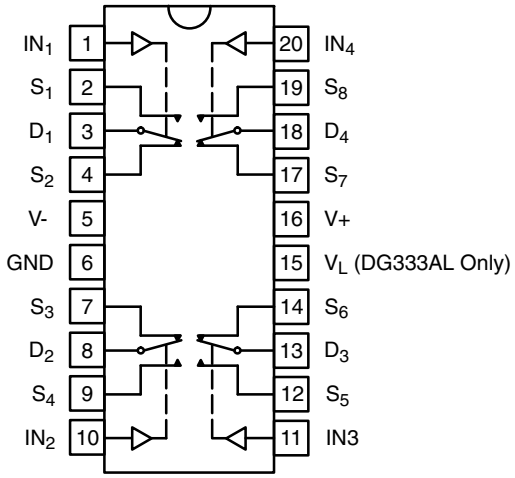
DESCRIPTION

The DG333A, DG333AL consist of four independently controlled single-pole double-throw analog switches. These monolithic switch is designed to control analog signals with a high degree of accuracy. The DG333A, DG333AL minimize measurement errors by offering low on-resistance (25 Ω typ), low leakage (20 pA typ.) and low charge injection performance. The DG333AL features micro-power operation (< 1 µW typ.). This is ideal for battery operated systems. Pin 15 is not connected on the DG333A.

An improved charge injection compensation design minimizes switching transients. These switches can handle up to ± 22 V signals and have an improved continuous current of 30 mA.

The DG333A, DG333AL is fabricated in Vishay Siliconix's proprietary HVSG-2 CMOS process, resulting in higher speed and lower power consumption. An epitaxial layer prevents latchup. Each switch conducts equally well in both directions when on. When off, they block voltages up to the power-supply levels.

DUAL-IN-LINE, WIDE-BODY SOIC AND TSSOP



Top View

FEATURES

- ± 22 V supply voltage range
- TTL and CMOS compatible logic
- Low on-resistance (25 Ω)
- On-resistance matched between channels (< 2 Ω)
- Flat on-resistance over analog signal range (Δ < 3 Ω)
- Low charge injection (1 pC)
- Low leakage (0.2 nA)
- Fast switching (175 ns)
- Single-supply operation (5 V to 40 V)
- ESD tolerance > 2 kV per 3015.x
- Low power (< 1 µA) - DG333A, DG333AL

BENEFITS

- Rail-to-rail analog signal range
- Simple logic interface
- High precision and accuracy
- Minimal transients
- Low distortion
- Reduced power consumption
- Improved reliability
- Break-before-make switching action

APPLICATIONS

- Audio switching
- Test equipment
- Portable instrumentation
- Communication systems
- PBX, PABX
- Computer peripherals
- Mass storage systems
- Switched-capacitor networks
- Battery-powered systems

TRUTH TABLE		
LOGIC	SW1, 4, 5, 8 NORMALLY OPEN	SW2, 3, 6, 7 NORMALLY CLOSED
0	OFF	ON
1	ON	OFF

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER [a]
-40 °C to +85 °C	20-Pin Plastic DIP	DG333ADJ-E3
		DG333ALDJ-E3
	20-Pin Wide-Body SOIC (shipped in tubes)	DG333ADW-E3
		DG333ALDW-E3
	20-Pin Wide-Body SOIC (shipped in tape and reel)	DG333ADW-T1-E3
		DG333ALDW-T1-E3
	20-Pin TSSOP (shipped in tape and reel)	DG333ADQ-T1-E3
		DG333ALDQ-T1-E3

Note

a. For standard tin / lead external termination, remove the "-E3" from the ordering part number.

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Voltages Referenced V+ to V-		44	V
GND		30	
V+ to GND		40	
Digital Inputs [a] V_S, V_D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current, Any Terminal		30	mA
Peak Current S or D (Pulsed at 1 ms, 10 % Duty Cycle max.)		100	
Storage Temperature		-65 to +125	°C
Power Dissipation (Package) [b]	20-Pin Plastic DIP [c]	890	mW
	20-Pin Wide SOIC [d]	800	

Notes

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 12 mW/°C above 75 °C.
d. Derate 10 mW/°C above 75 °C.

SCHEMATIC DIAGRAM (Typical Channel)

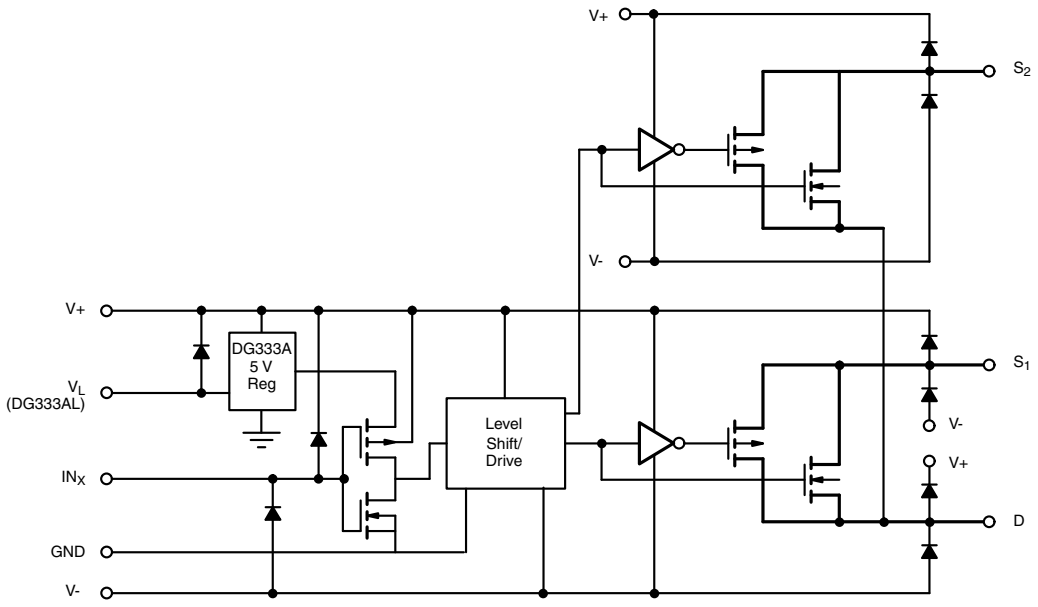


Fig. 1

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = -15 V V_{IN} = 2.4 V or 0.8 V [e]	TEMP. [a]	LIMITS D SUFFIX -40 °C to +85 °C MIN. [b]	TYP. [c]	MAX. [b]	UNIT
Analog Switch							
Analog Signal Range [d]	V_{ANALOG}		Full	V-	-	V+	V
Channel On-Resistance	$R_{DS(on)}$	I_S = -10 mA, V_D = ± 10 V	Room	-	25	45	Ω
			Full	-	-	90	
On-Resistance Flatness		I_S = -10 mA, V_D = ± 5 V V+ = 16.5 V, V- = -16.5 V	Room	-	-	3	
			Full	-	-	5	
$R_{DS(on)}$ Match Between Channels [f]	$\Delta R_{DS(on)}$	I_S = -10 mA, V_D = ± 10 V	Room	-	-	2	
			Full	-	-	4	
Source Off Leakage Current	$I_{S(off)}$	V_D = 15.5 V, V_S = 15.5 V V+ = 16.5 V, V- = -16.5 V	Room	-0.25	-	0.25	nA
			Hot	-20	-	20	
Channel On Leakage Current	$I_{D(on)}$	V_D = ± 15.5 V, $V_{S(open)}$ = ± 15.5 V V+ = 16.5 V, V- = -16.5 V	Room	-0.75	-	0.75	
			Hot	-60	-	60	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4	-	-	V
Input Voltage Low	V_{INL}		Full	-	-	0.8	
Input Current	I_{INL} or I_{INH}	V_{INH} or V_{INL}	Full	-1	-	1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	See switching time test circuit see figure 2	Room	-	-	175	ns
Turn-Off Time	t_{OFF}		Room	-	-	145	
Break-Before-Make Time Delay	t_D	See figure 3	Room	5	-	-	
Charge Injection [d]	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	-	-	10	pC
Off-Isolation	OIRR	R_L = 75 Ω, C_L = 5 pF V_D = 2.3 V_{RMS}, f = 1 MHz	Room	-	72	-	dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	-	80	-	
Off Capacitance	C_{OFF}	f = 1 MHz, V_S = 0 V	Room	-	8	-	pF
Channel On Capacitance	C_{ON}		Room	-	12	-	
Power Supplies							
Positive Supply Current	I+	DG333A: V_{IN} = 0 V or 5 V	Room	-	-	200	µA
Negative Supply Current	I-		Room	-1	-	-	
Positive Supply Current	I+	DG333AL: V_{IN} = 0 V or 5 V, V_L = 5 V	Room	-	-	1	
Logic Supply Current	I_L		Room	-	-	1	
Negative Supply Current	I-		Room	-1	-	-	
Supply Voltage Range	V+/V-		Full	± 4	-	± 22	V

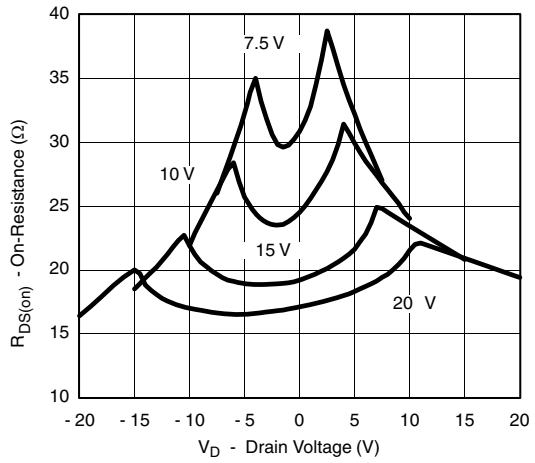
SPECIFICATIONS (Unipolar Supplies)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 12 V, V- = 0 V T_A = 25°C	**TEMP.** [a]	**LIMITS D SUFFIX** -40 °C to +85°C			**UNIT**
				MIN. [b]	**TYP.** [c]	**MAX.** [b]	
Analog Switch							
Analog Signal Range [d]	V_{ANALOG}		Full	V-	-	V+	V
Channel On-Resistance	$R_{DS(on)}$	I_S = -10 mA, V_D = 10, 1 V	Room	-	35	75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_D = 11 V, $V_{S(open)}$ = 1 V	Room	-	-	0.25	nA
Channel On Leakage Current	$I_{D(on)}$	V_D = 11 V, $V_{S(open)}$ = 0 V V_D = 1 V, $V_{S(open)}$ = V+	Room	-	-	0.75	
Dynamic Characteristics							
Turn-On Time	t_{ON}	See switching time test circuit see figure 2	Room	-	90	-	ns
Turn-Off Time	t_{OFF}		Room	-	45	-	
Break-Before-Make Time Delay	t_D	See figure 3	Room	5	10	-	
Power Supplies							
Positive Supply Current	I+	DG333A: V_{IN} = 0 V or 5 V	Room	-	-	200	µA
			Room	-	-	1	
Positive Supply Current	I+	DG333AL: V_{IN} = 0 V or 5 V, V_L = 5 V	Room	-	-	1	
Logic Supply Current	I_L		Room	-	-	1	
Positive Supply Range	V+		Room	5	-	40	V

Notes

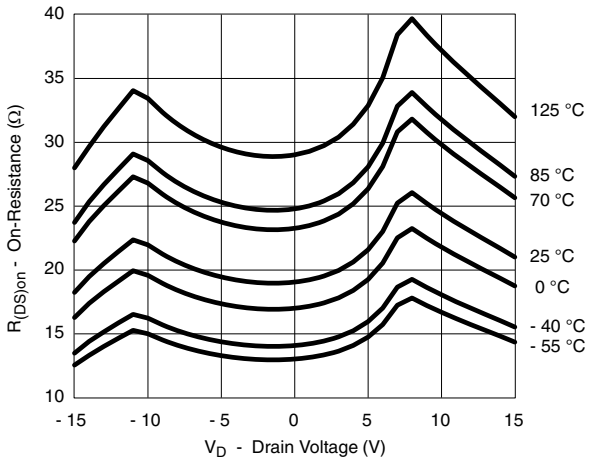
a. Room = 25 °C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.
f. On-resistance match and flatness are guaranteed only for bipolar supply operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

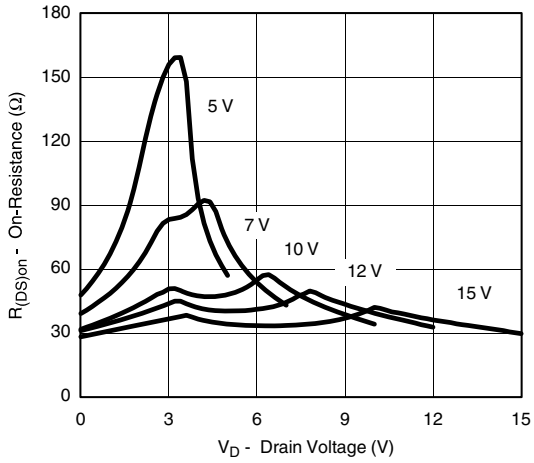


$R_{DS(on)}$ vs. V_D (Dual Supply)

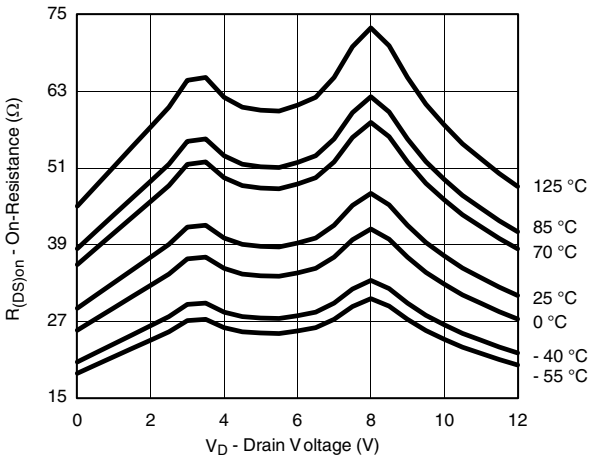


$R_{DS(on)}$ vs. V_D and Temperature (Dual Supply)

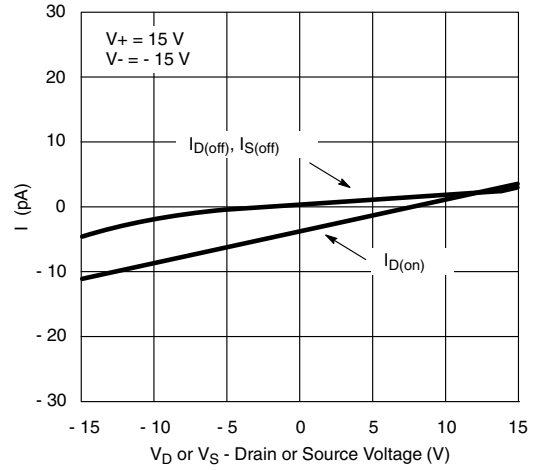
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



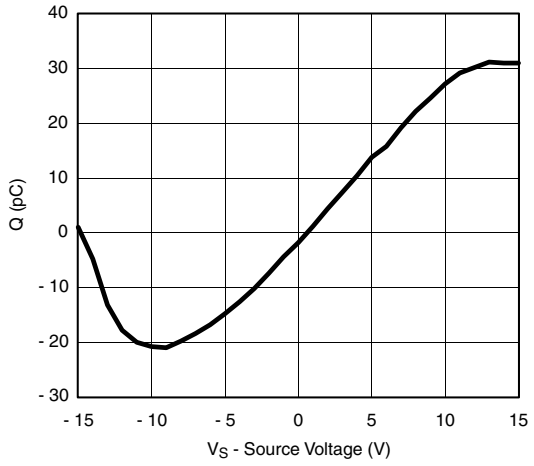
$R_{DS(on)}$ vs. V_D (Single Supply)



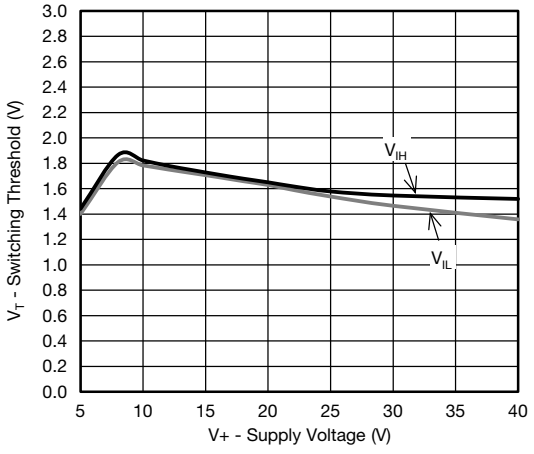
$R_{DS(on)}$ vs. V_D and Temperature (Single Supply)



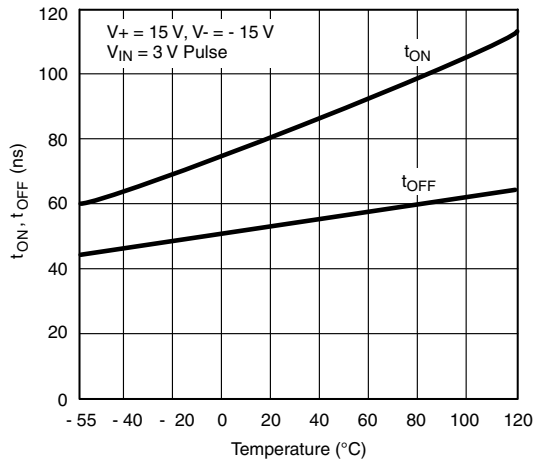
Leakage Current vs. Analog Voltage



Drain Charge Injection

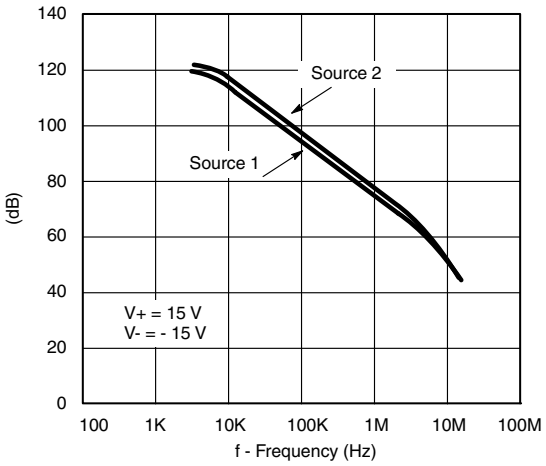


Input Switching Threshold vs. Supply Voltage

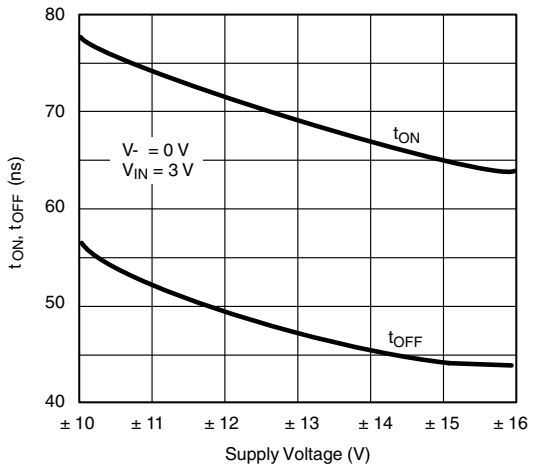


Switching Time vs. Temperature

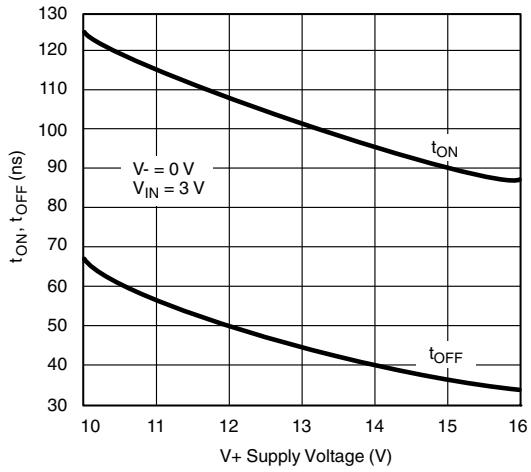
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



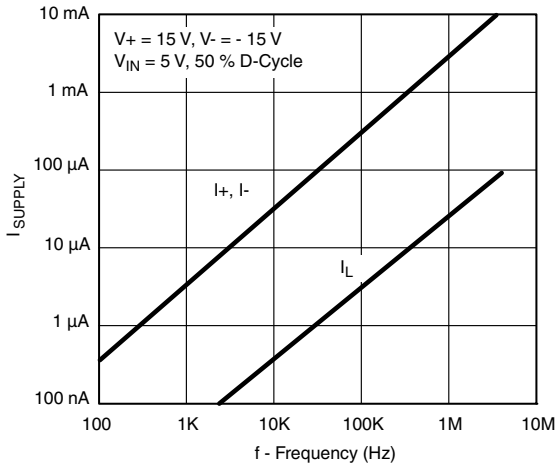
Crosstalk and Off Isolation vs. Frequency



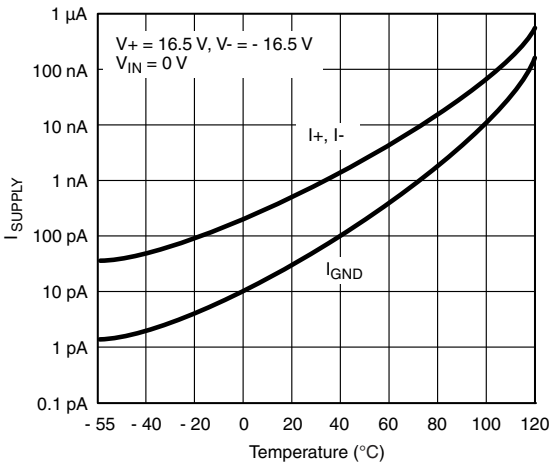
Switching Time vs. Supply Voltages



Switching Time vs. V+

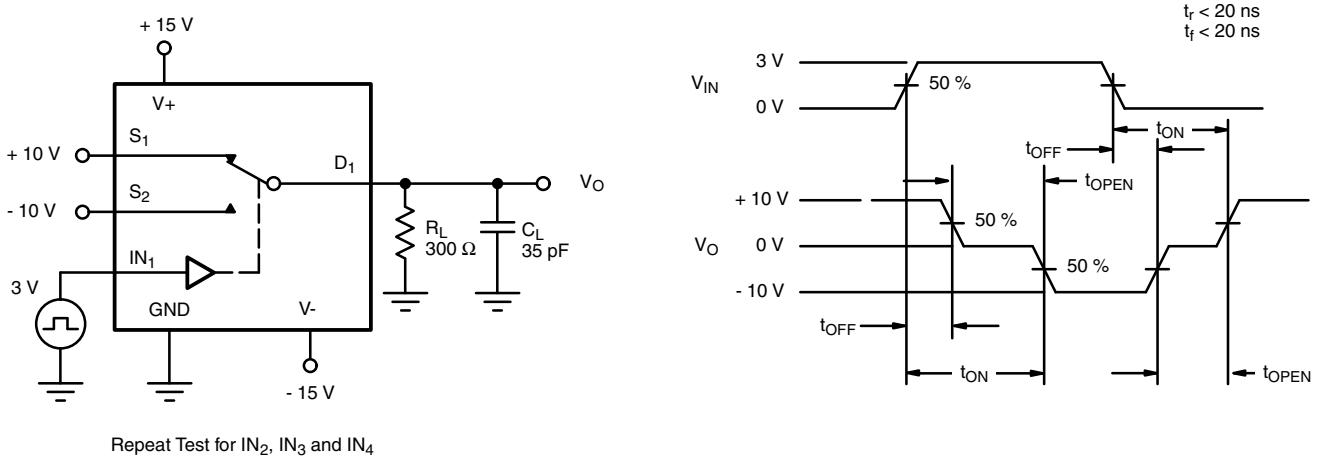


Power Supply Currents vs. Switching Frequency



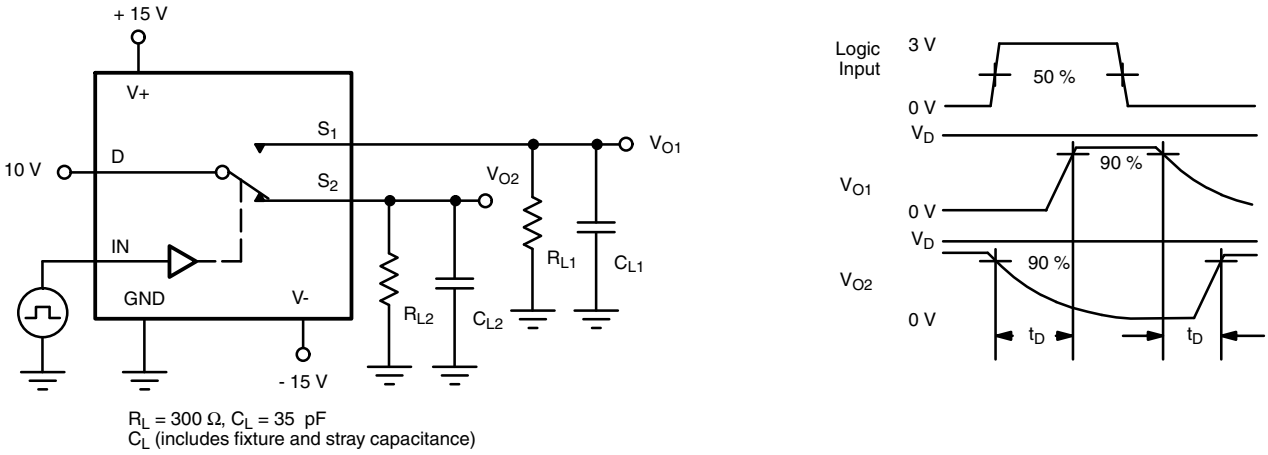
Supply Current vs. Temperature

TEST CIRCUITS



Repeat Test for IN_2, IN_3 and IN_4

Fig. 2 - Switching Time



R_L = 300 Ω, C_L = 35 pF
C_L (includes fixture and stray capacitance)

Fig. 3 - Break-Before-Make

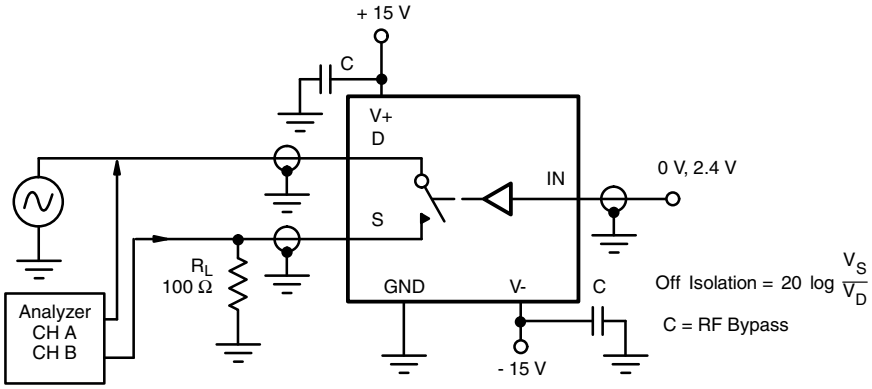


Fig. 4 - Off Isolation

TEST CIRCUITS

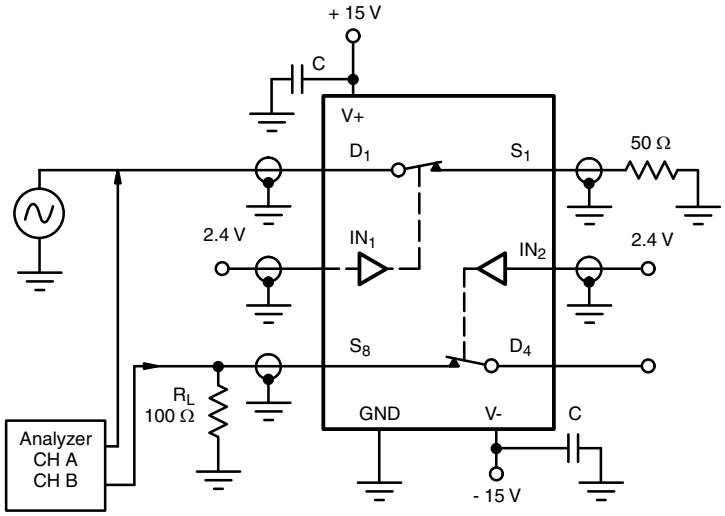


Fig. 5 - Crosstalk

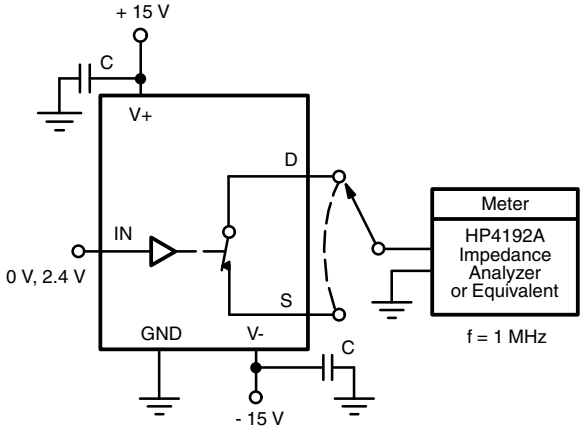


Fig. 6 - Capacitances

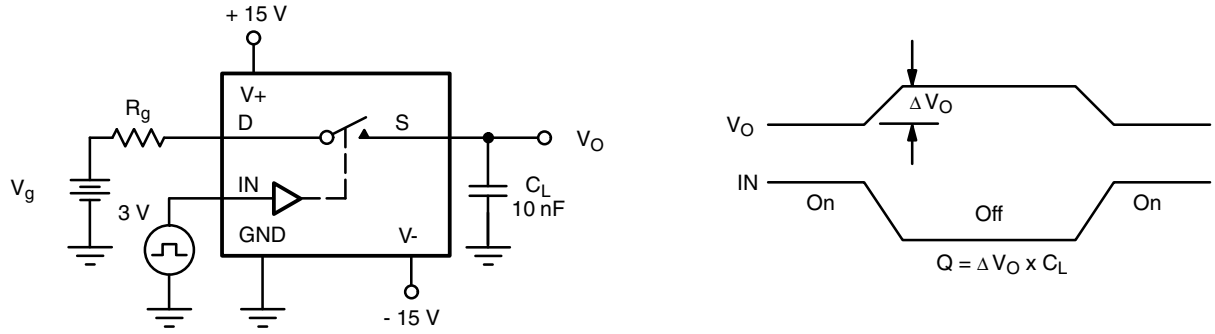


Fig. 7 - Charge Injection

APPLICATIONS

Band-Pass Switched Capacitor Filter

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG333A, DG333AL allow for higher clock rates and consequently higher filter operating frequencies. Figure 8 shows two capacitors being switched.

The DG333A, DG333AL is capable of switching four capacitors.

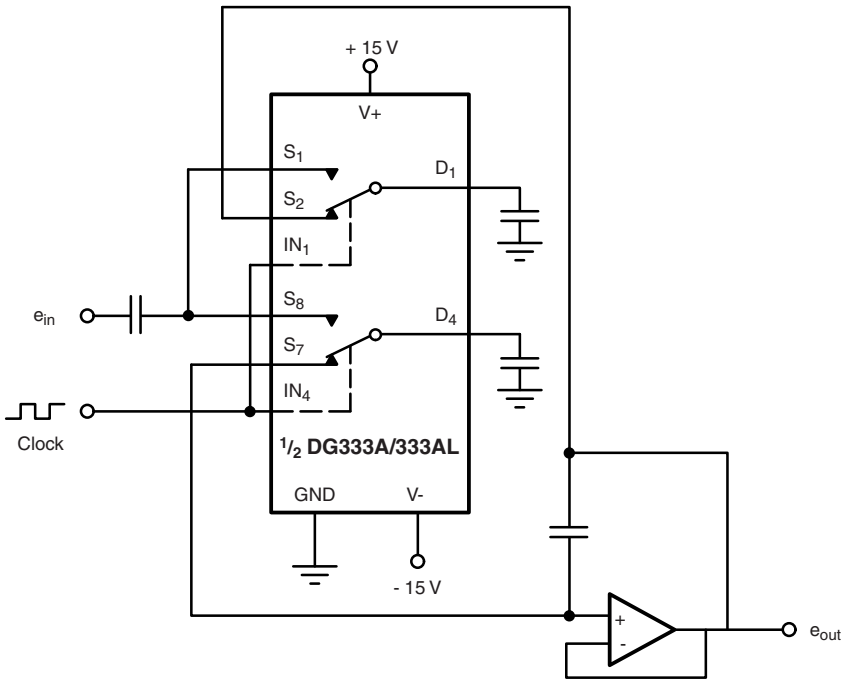
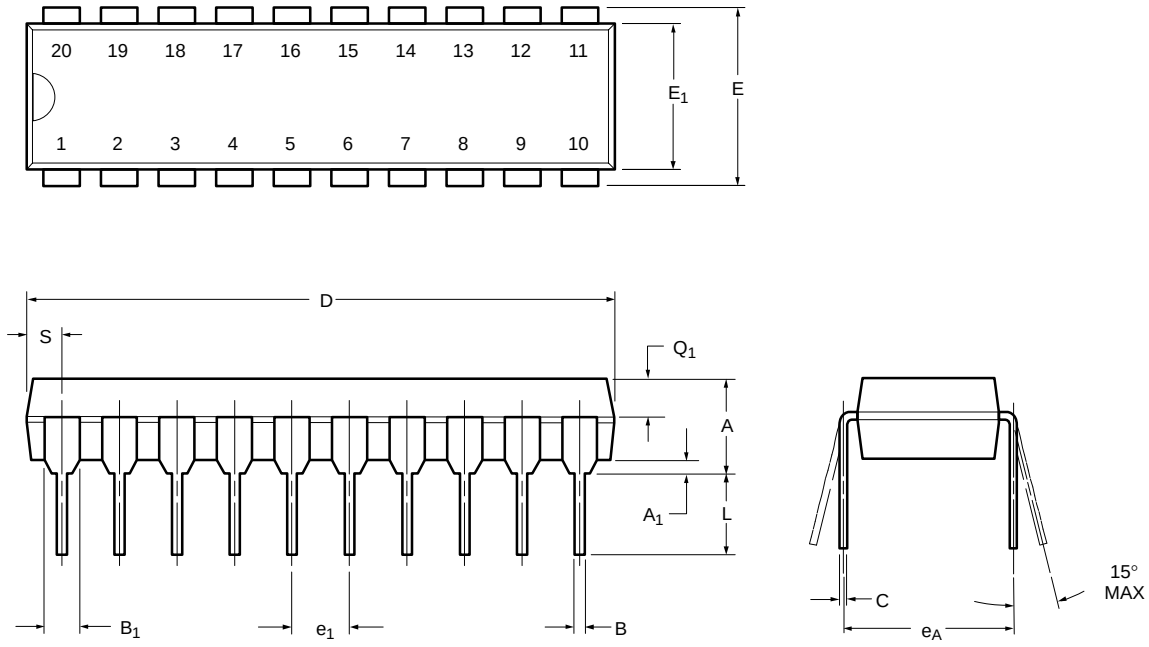


Fig. 8 - Band-Pass Switched Capacitor Filter

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70803.

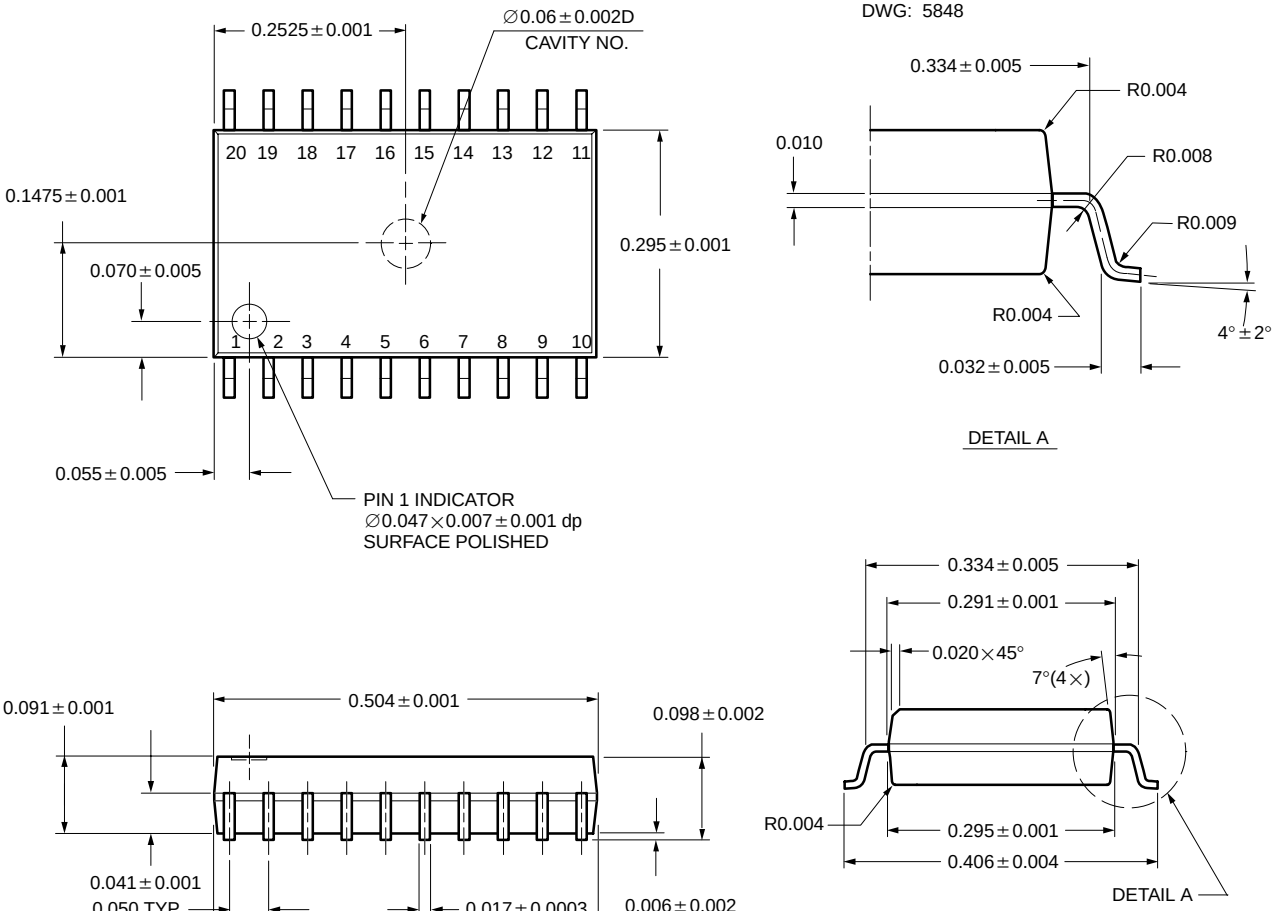
PDIP: 20-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	24.89	26.92	0.980	1.060
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	3.175	3.81	0.123	0.150
Q_1	1.27	2.03	0.050	0.080
S	1.02	2.03	0.040	0.080
ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5484				

SOIC (WIDE-BODY): 20-LEAD

ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5848



All Dimensions In Inches.

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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